About this Manual

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HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. In other documentation, to reduce potential confusion, the only change to product numbers and names has been in the company name prefix: where a product number/name was HP XXXX the current name/number is now Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

User's Guide

Publication Number 01660-97023
First Edition, November 1997

For Safety Information, Warranties, and Regulatory Information, see the pages at the end of this manual.

HP 1660CP-Series Logic Analyzers

HP 1660CP-Series Logic Analyzers

The HP 1660CP-Series are 100-MHz State/500-MHz Timing Logic Analyzers.

Logic Analyzer Features

- 130 data channels and 6 clock/data channels in the HP 1660CP
- 96 data channels and 6 clock/data channels in the HP 1661CP
- 64 data channels and 4 clock/data channels in the HP 1662CP
- 32 data channels and 2 clock/data channels in the HP 1663CP
- 3.5-inch flexible disk drive and 540 MB hard disk drive
- HP-IB and RS-232-C controller and printer interface, Centronics printer interface
- Variable setup/hold time
- 4 K memory on all channels with 8 K in half-channel mode
- Marker measurements
- 12 levels of trigger sequencing for state and 10 levels of trigger sequencing for timing
- 100 MHz time tagging and number-of-states tagging
- Full programmability
- DIN mouse and keyboard support

Pattern Generator Features

- 16 output channels at 200 MHz
- 32 output channels at 100 MHz
- 258,048 vectors
- 3-bit pattern-level sensing (clock pod)

Options include the Programmer's Guide and the Service Guide.

In This Book

This User's Guide shows you how to use the HP 1660CP-Series Logic Analyzer. It contains measurement examples, field and feature definitions, and a basic service guide. Refer to this manual for information on what the menu fields do and how they are used. This manual covers all HP 1660CP-series analyzers.

The User's Guide is divided into four parts. The first part, chapters 1 through 5, covers general product information you need to use the logic analyzer. The second part, chapters 6 and 7, contains detailed examples to help you use your analyzer in performing complex measurements. The third part, chapters 8 through 10, contains reference information on the hardware and software, including the analyzer menus and how they are used. There are sections for each analyzer menu and a separate chapter on System Performance Analysis. The fourth part, chapters 11 through 13, provides a basic service guide.

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4 Using the Trigger Menu

5 Using the Pattern Generator

10 Concepts

11 Troubleshooting

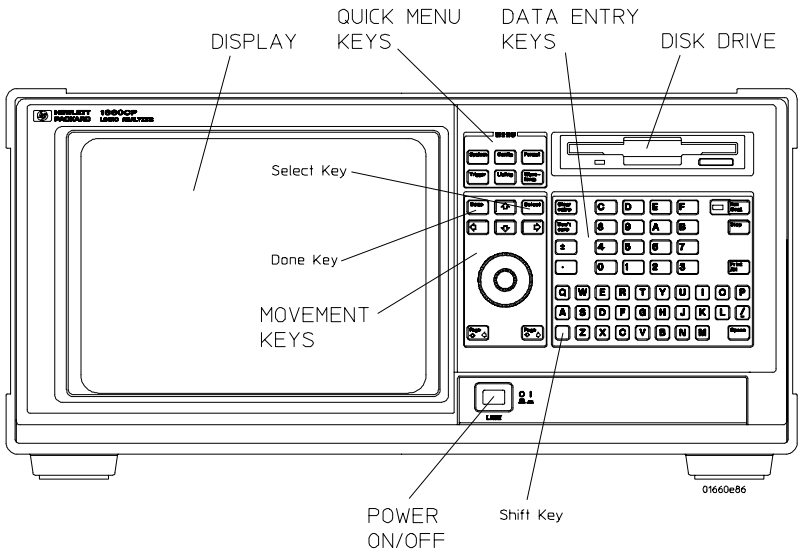
12 Specifications

13 Operator's Service

1

Logic Analyzer Overview

HP 1660CP-Series Logic Analyzer



HP 1660CP-Series Logic Analyzer Front Panel

Select Key

The Select key action depends on the type of field currently highlighted. If the field is an option field, the Select key brings up an option menu or, if there are only two possible values, toggles the value in the field. If the highlighted field performs a function, the Select key starts the function.

Done Key

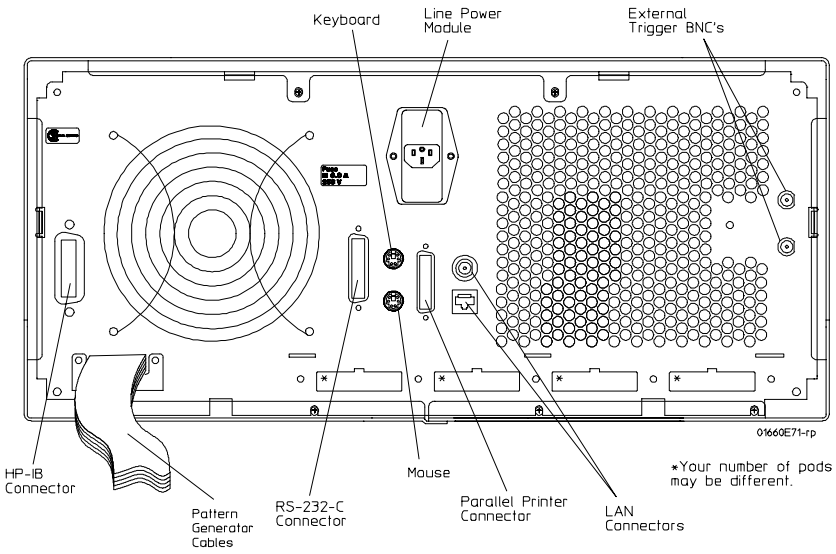
The Done key saves assignments and closes pop-up menus. In some fields, its action is the same as the Select key.

Shift Key

The shift key, which is blue, provides lowercase letters and access to the functions in blue on some of the keys. You do not need to hold the shift key down while pressing the other key — just press the shift key first, and then the function key.

Knob

The knob can be used in some fields to change values. These fields are indicated by a side view of the knob placed on top of the field when it is selected. The knob also scrolls the display and moves the cursor within lists. If you are using a mouse, you can do the same actions by holding down the right button of the mouse while dragging.



HP 1660CP-Series Logic Analyzer Back Panel

Line Power Module

Permits selection of 110-120 or 220-240 Vac and contains the fuses for each of these voltage ranges.

External Trigger BNCs

The External Trigger BNCs provide the "Port In" and "Port Out" connections for the Arm In and Arm Out of the Trigger Arming Control menu.

RS-232-C Connector
Standard DB-25 type connector for connecting an RS-232-C printer or controller.

HP-IB Connector
Standard HP-IB connector for connecting an HP-IB printer or controller.

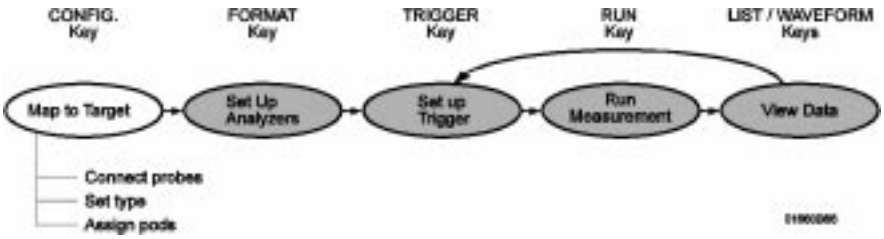
Parallel Printer Connector
Standard Centronics connector for connecting a parallel printer.

LAN Connectors
Connects the logic analyzer to your local ethernet network. The BNC connector on top accepts 10Base2 ("thinlan"). The UTP connector below the BNC connector accepts 10Base-T ("ethertwist").

To make a measurement

For more detail on any of the information below, see the referenced chapters or the Logic Analyzer Training Kit. If you are using a preprocessor with the logic analyzer, some of these steps may not apply.

Map to target



Connect probes Connect probes from the target system to the logic analyzer to physically map the target system to the channels in the logic analyzer. Attach probes to a pod in a way that keeps logically-related channels together. Remember to ground the pod.

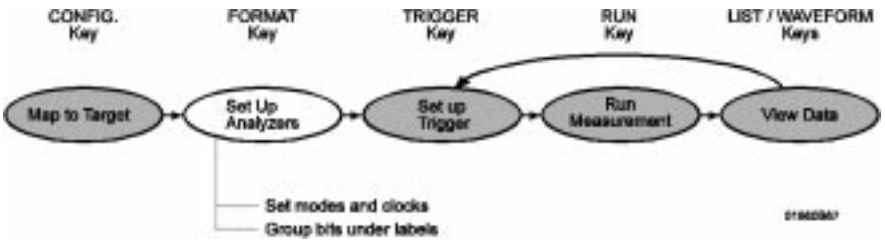
See Also "Probing" in Chapter 8 for more detail on constructing probes.

Set type* When the logic analyzer is turned on, Analyzer 1 is named Machine 1 and is configured as a timing analyzer, and Analyzer 2 is off. To use state analysis or software profiling, you must set the type of the analyzer in the Analyzer Configuration menu. You can only use one timing analyzer at a time.

Assign pods* In the Analyzer Configuration menu, assign the connected pods to the analyzer you want to use. The number of pods on your logic analyzer depends on the model. Pods are paired and always assigned as a pair to a particular analyzer.

* If you load a configuration file, this step is not necessary.

Set up analyzers*



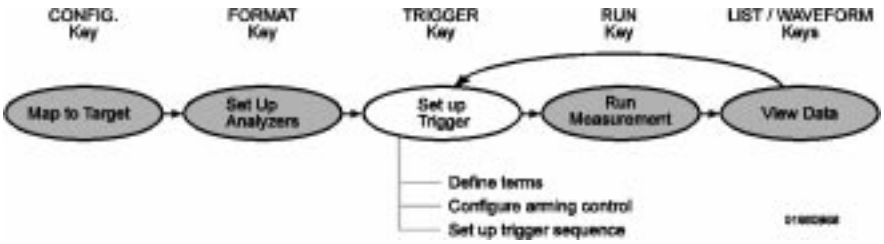
Set modes and clocks Set the state and timing analyzers using the Analyzer Format menu. In general, these modes trade channel count for speed or storage. The state analyzer also provides for complicated clocking. If your state clock is set incorrectly, the data gathered by the logic analyzer might indicate an error where none exists.

See Also "The Analyzer Format Menu" in Chapter 8 for more information on modes and clocks.

Group bits under labels The Analyzer Format menu indicates active pod bits. You can create groups of bits across pods or subgroups within pods and name the groups or subgroups using labels.

* If you load a configuration file, this step is not necessary.

Set up trigger



Define terms In the Analyzer Trigger menu, define trigger variables called terms to match specific conditions in your target system. Terms can match patterns, ranges, or edges across multiple labels.

Configure Arming Control Use Arming Control if

- you want to correlate the triggers and data of both analyzers
- you want to use the logic analyzer to trigger an external instrument, or
- you want to use an external instrument to trigger the logic analyzer.

Set up trigger sequence Create a sequence of steps that control when the logic analyzer starts and stops storing data and filters which data it will store. For common tasks, you can use a trigger macro to simplify the process or use the user-defined macros to loop and jump in sequence.

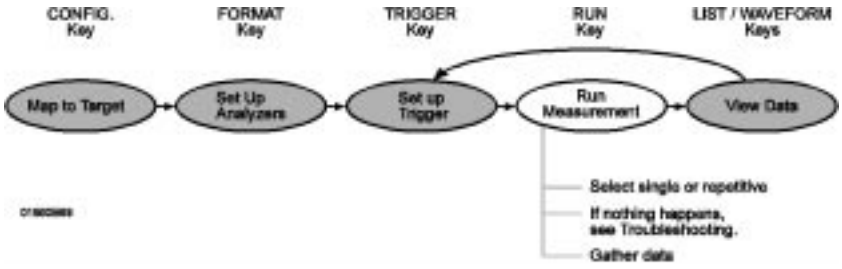
See Also

Chapter 4,"Using the Trigger Menu" and Chapter 6, "Triggering Examples" for more information on setting up a trigger.

"The Trigger Sequence" in Chapter 10 for more information about the trigger sequence mechanism.

"To save a configuration" and "To load a configuration" in Chapter 7 for instructions on saving and loading the setup so you don't have to repeat setting up the analyzer and trigger.

Run measurement



Select single or repetitive From any Analyzer menu, select the field labeled Run in the upper right corner to start measuring, or press the Run key. A single run will run once, until memory is full; a repetitive run will go until you select Stop or until a stop measurement condition that you set in the markers menu is fulfilled.

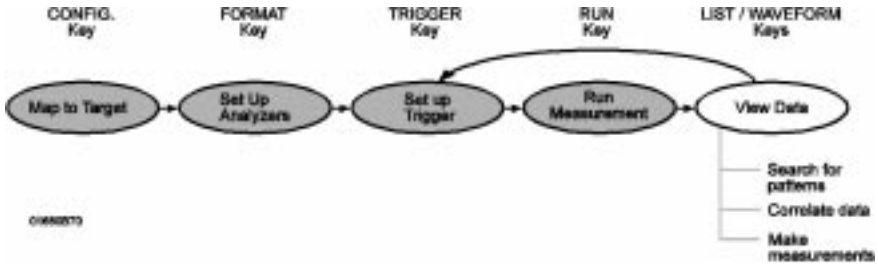
See Also

"Markers" sections in Chapter 8 for more information on markers and stop measurement conditions.

If nothing happens, see Troubleshooting. When you start a run, your analyzer menu changes to one of the display menus or a status message pops up. If nothing happens, press the Stop key or select Cancel. If the analyzer still does not display any measurements, see Chapter 11, "Troubleshooting."

Gather data You can gather statistics automatically by going to the Waveform or Listing menu, turning on markers, and setting patterns for the X and O markers. You can set the analyzer to stop if certain conditions are exceeded, or just use the markers to count valid runs.

View data



Search for patterns In both the Waveform and Listing menus you can use symbols and markers to search for patterns in your data. In the Analyzer Waveform or Analyzer Listing menu, toggle the Markers field to turn the pattern markers on and then specify the pattern. When you switch views, the markers keep their settings.

Correlate data You can correlate data by setting Count Time in your state analyzer's Trigger menu and then using interleaving and mixed display. Interleaving correlates the listings of two state analyzers. Mixed display correlates a timing analyzer waveform and a state analyzer listing. The System Performance Analysis (SPA) Software does not save a record of actual activity, so it cannot be correlated with either timing or state mode.

Make measurements The markers can count occurrences of events, measure durations, and collect statistics, and SPA provides high-level summaries to help you identify bottlenecks. To use the markers, select the appropriate marker type in the display menu and specify the data patterns for the marker. To use SPA, go to the SPA menu, select the most appropriate mode, fill in the parameters, and press Run.

See Also

Chapter 9, "System Performance Analysis (SPA) Software" for more information on using SPA.

"The Waveform Menu" and "The Listing Menu" in Chapter 8 for additional information on the menu features.

2

Connecting Peripherals

Connecting Peripherals

Your HP 1660CP-series logic analyzer comes with a PS2 mouse. It also provides connectors for a keyboard, Centronics (parallel) printer, and HP-IB and RS-232-C devices. This chapter tells you how to connect peripheral equipment such as the mouse or a printer to the logic analyzer.

Mouse and Keyboard

You can use either the supplied mouse and optional keyboard, or another PS2 mouse and keyboard with standard DIN connector. The DIN connector is the type commonly used by personal computer accessories.

Printers

The logic analyzer communicates directly with HP PCL printers supporting the printer control language or with other printers supporting the Epson standard command set. Many non-Epson printers have an Epson-emulation mode. HP PCL printers include the following:

- HP ThinkJet
- HP LaserJet
- HP PaintJet
- HP DeskJet
- HP QuietJet

You can connect your printer to the logic analyzer using HP-IB, RS-232-C, or the parallel printer port. The logic analyzer can only print to printers directly connected to it. It cannot print to a networked printer.

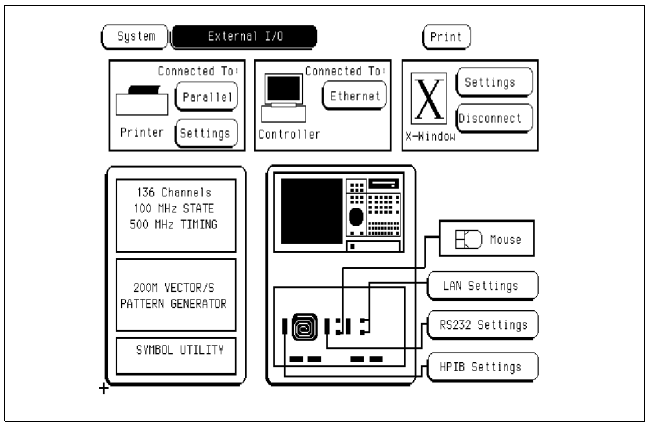
To connect a mouse

Hewlett-Packard supplies a mouse with the logic analyzer. If you prefer a different style of mouse you can use any PS2 mouse with a standard PS2 DIN interface.

1. **Plug the mouse into the mouse connector on the back panel. Make sure the plug shows the arrow on top.**
2. **To verify connection, check the System External I/O menu for a mouse box.**

   The mouse box is on the right side above the Settings fields. If the logic analyzer was displaying the System External I/O menu when you plugged in the mouse, the menu won't update until you exit and then return to it.

   The mouse pointer looks like a plus sign (+). To select a field, move the pointer over it and press the left button. To duplicate the front-panel knob, hold down the right button while moving the mouse. Moving the mouse up or to the right duplicates turning the knob clockwise. Moving the mouse down or to the left duplicates turning the knob counterclockwise.



System External I/O Menu Showing Mouse Installed

To connect a keyboard

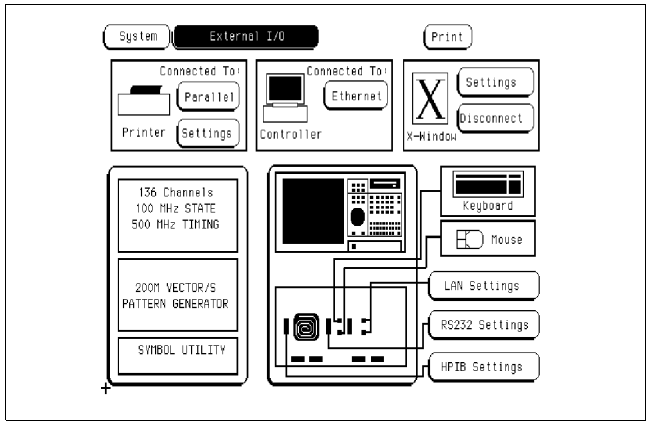
You can use either the HP-recommended keyboard, HP E2427B, or any other keyboard with a standard DIN connector.

1. **Plug the keyboard into the keyboard connector on the back panel.**
2. **To verify, check the System External I/O menu for a keyboard box.**

   The keyboard box is on the right side, above the Settings fields. If the logic analyzer was displaying the System External I/O menu while you plugged the keyboard in, the menu won't update until you exit and then return to it.

   The keyboard cursor is the location on the screen highlighted in inverse video. To move the cursor, use the arrow keys. Pressing Enter selects the highlighted field. The primary keyboard keys act like the analyzer's front-panel data entry keys.

See Also "Keyboard Shortcuts" in the Chapter 8 for complete key mappings.



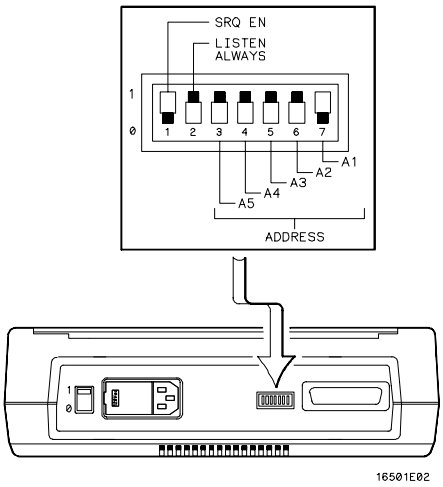
System External I/O Menu Showing Keyboard Installed

To connect to an HP-IB printer

Printers connected to the logic analyzer over HP-IB must support HP-IB and Listen Always. When controlling a printer, the analyzer's HP-IB port does not respond to service requests (SRQ), so the SRQ enable setting does not have any effect on printer operation.

1. Turn off the analyzer and the printer, and connect an HP-IB cable from the printer to the HP-IB connector on the analyzer rear panel.
2. Turn on the analyzer and printer.
3. Make sure the printer is set to **Listen Always** or **Listen Only**.

   For example, the figure below shows the HP-IB configuration switches for an HP-IB ThinkJet printer. For the Listen Always mode, move the second switch from the left to the 1 position. Because the instrument doesn't respond to SRQ EN (Service Request Enable), the position of the first switch doesn't matter.



Listen AlwaysSwitchSetting

4 Go to the System External I/O menu and configure the analyzer's printer settings.

a If the analyzer is not already set to HP-IB, select the field under Connected To: in the Printer box and choose HP-IB from the menu.

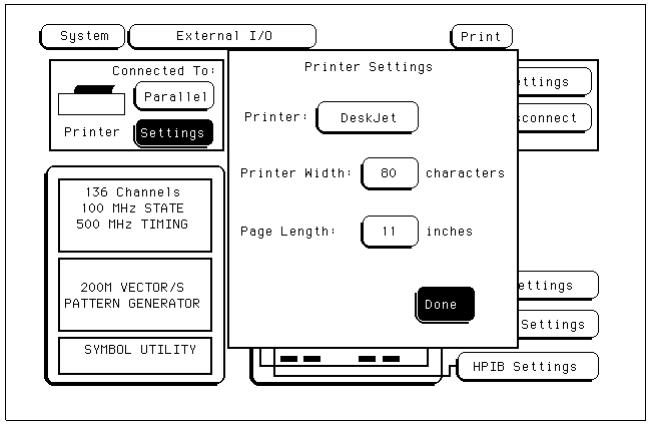
b Select the Printer Settings field.

c In the top field of the pop-up, select the type of printer you are using. If you are using an Epson graphics printer or an Epson-compatible printer, select Alternate.

d If the default print width and page length are not what you want, select the fields to toggle them.

If you select 132 characters per line when using a printer other than QuietJet, the listings are printed in a compressed mode. QuietJet printers can print 132 characters per line without going to compressed mode, but require wider paper.

e Press Done.



Printer Settings menu

To connect to an RS-232-C printer

1. Turn off the analyzer and the printer, and connect a null-modem RS-232-C cable from the printer to the RS-232-C connector on the analyzer rear panel.
2. Before turning on the printer, locate the mode configuration switches on the printer and set them as follows:
   - For the HP QuietJet series printers, there are two banks of mode function switches inside the front cover. Push all the switches down to the 0 position.
   - For the HP ThinkJet printer, the mode switches are on the rear panel of the printer. Push all the switches down to the 0 position.
   - For the HP LaserJet printer, the factory default switch settings are okay.
3. Turn on the analyzer and printer.
4. Go to the System External I/O menu and configure the analyzer's printer settings.
   a. If the analyzer is not already set to RS232, select the field under Connected To: in the Printer box and choose RS232 from the menu.
   b. Select the Printer Settings field.
   c. In the top field of the pop-up, select the type of printer you are using. If you are using an Epson graphics printer or an Epson-compatible printer, select Alternate.
   d. If the default print width and page length are not what you want, select the fields to toggle them.

      If you select 132 characters per line when using a printer other than QuietJet, the listings are printed in a compressed mode. QuietJet printers can print 132 characters per line without going to compressed mode, but require wider paper.
   e. Press Done.
5. Select the RS232 Settings field and check that the current settings are compatible with your printer.

See Also

"The RS-232-C, HP-IB, and Centronics Interface" section in Chapter 8 for more information on RS-232-C settings.

To connect to a parallel printer

1. Turn off the analyzer and the printer, and connect a parallel printer cable from the printer to the parallel printer connector on the analyzer rear panel.
2. Before turning on the printer, configure the printer for parallel operation.

   The printer's documentation will tell you what switches or menus need to be configured.
3. Turn on the analyzer and printer.
4. Go to the System External I/O menu and configure the analyzer's printer settings.
   a. If the analyzer is not already set to Parallel, select the field under Connected To: in the Printer box and choose Parallel from the menu.
   b. Select the Printer Settings field.
   c. In the top field of the pop-up, select the type of printer you are using. If you are using an Epson graphics printer or an Epson-compatible printer, select Alternate.
   d. If the default print width and page length are not what you want, select the fields to toggle them.

      If you select 132 characters per line when using a printer other than QuietJet, the listings are printed in a compressed mode. QuietJet printers can print 132 characters per line without going to compressed mode, but require wider paper.
   e. Press Done.

There are no settings specific to the parallel printer connector.

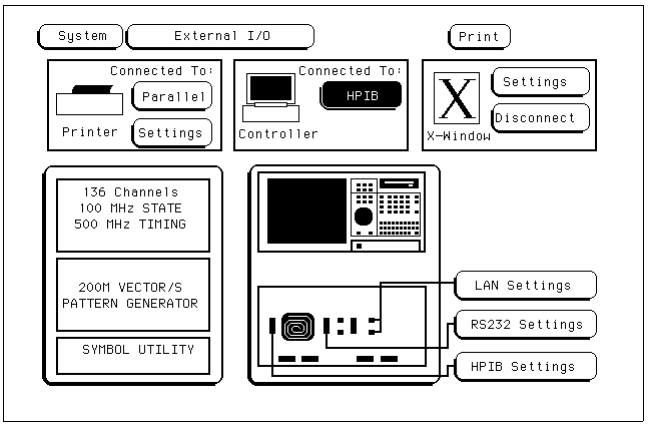
To connect to a controller

You can control the HP 1660CP-series logic analyzer with another instrument, such as a computer running a program with embedded analyzer commands. The steps below outline the general procedure for connecting to a controller using HP-IB or RS-232-C.

1. **Turn off both instruments, and connect the cable.**

   If you are using RS-232-C, the cable must be a null-modem cable. If you do not have a null-modem cable, you can purchase an adapter at any electronics supply store.

2. **Turn on the logic analyzer and then the controller.**
3. **In the System External I/O menu, select the field under Connected To: in the Controller box and set it appropriately.**
4. **Select the appropriate Settings field and configure the values in the pop-up menu to be compatible with the controller.**



HP-IB Connection

See Also

HP 1660C/CS/CP-Series Logic Analyzers Programmer's Guide and *LAN User's Guide* for more information on connecting controllers.

3

Using the Logic Analyzer

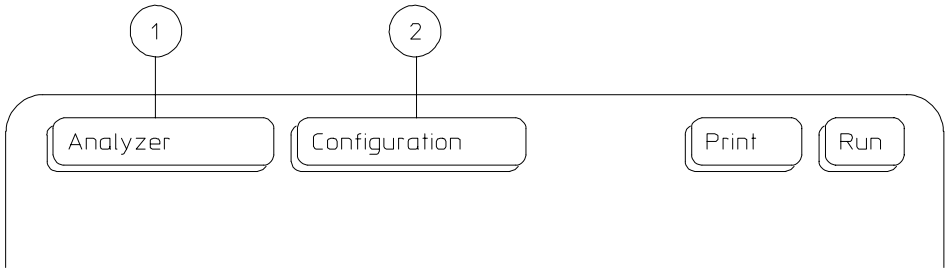
Using the Logic Analyzer

This chapter shows you how to perform the basic tasks necessary to make a measurement. Each section uses an example to show how the task fits into the overall goal of making a measurement.

Accessing the Menus

When you power up the logic analyzer, the first screen after the system tests is the Analyzer Configuration menu. Menus are identified by two fields in the upper left corner. The leftmost field shows Analyzer. This field is sometimes referred to as the "mode field" because it controls which other set of menus you can access. The second field, just to the right of the mode field, accesses menus within the mode and so is called the "menu field." For example, if you are in Analyzer mode, the menus for the analyzer are accessed from the menu field. Menus are referred to by the titles that appear in the mode and menu fields, for example, the Analyzer Configuration menu.

The figure below shows the top of the first screen. The mode field, item 1, displays "Analyzer." The menu field, item 2, displays "Configuration." Because menus are identified by the titles in these two fields, this menu is referred to as the Analyzer Configuration menu. When there is no risk of confusion, the menu is sometimes referred to just by the title showing in the second field, for example, the Configuration menu.



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To access the System menus

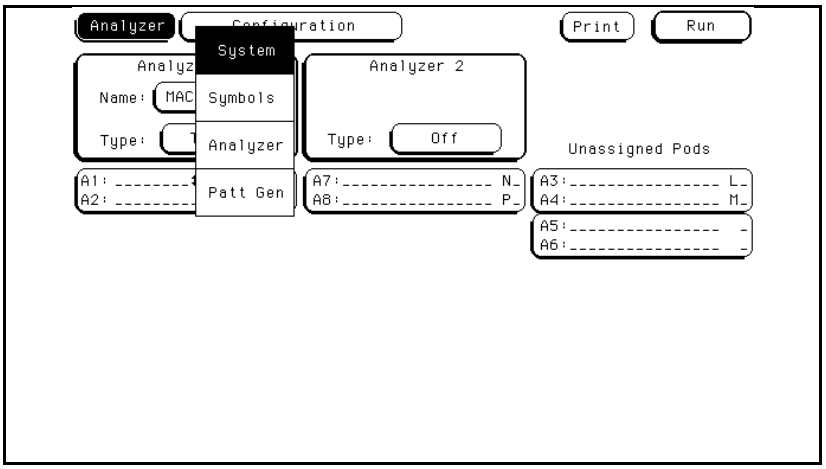
The System menus allow you to perform operations that affect the entire logic analyzer, such as load configurations, change shades, and perform system diagnostics.

1 Select the mode field.

Use the arrow keys to highlight the mode field, then press the Select key. Or, if you are using the mouse, click on the field. This operation is referred to as "select."

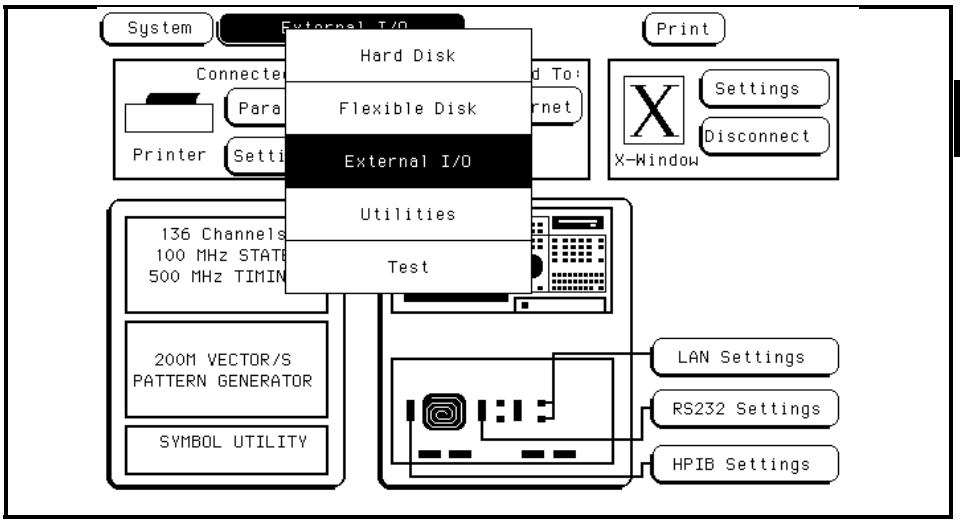
A pop-up menu appears with the choices System and Analyzer. (If you have installed any optional software, there may be other choices as well.)

2 Select System.



3 Select the menu field.

The pop-up lists five menus: Hard Disk, Flexible Disk, External I/O, Utilities, and Test.



- Hard Disk allows you to perform file operations on the hard disk.
- Flexible Disk allows you to perform file operations on the flexible disk.
- External I/O allows you to configure your HP-IB, RS-232-C, and LAN interfaces and connect to a printer and controller.
- Utilities allows you to set the clock, update the operating system software, and adjust the display.
- Test displays the installed software version number and loads the self tests.

See Also

For information on "File Management" see Chapter 7,and for information on "Disk Drive Operations" see Chapter 8.

For information on the External I/O menu, "Connecting Peripherals", see Chapter 2, and "The RS-232-C, HP-IB, and Centronics Interfaces" see Chapter 8.

For how to run the self-tests, "Operator's Service" see Chapter 13.

To access the Analyzer menus

The Analyzer menus allow you to control the analyzer to make your measurement, perform operations on the data, and view the results on the display.

1 Select the mode field.

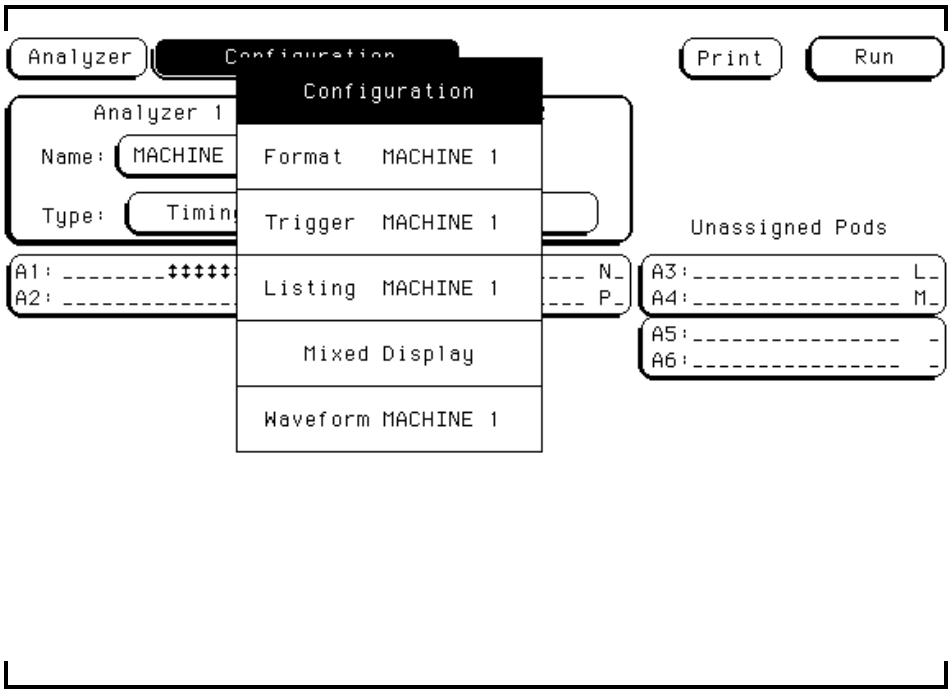
A pop-up menu appears with the choices System, Analyzer, and Patt Gen. (If you have installed any optional software, there may be other choices as well.)

2 Select Analyzer.

3 Select the menu field.

The figure on the next page does not show all of the possible menus because certain menus are only accessible with the analyzer configured in a particular mode. For instance, the Compare menu is only available when you set an analyzer to state mode, and the SPA menu requires an analyzer set to SPA.

- Configuration is always available in Analyzer mode. Use Configuration to assign pods and set the analyzer type.
- Format is available whenever an analyzer is set to a type other than "Off." Use Format to create data labels and symbols, adjust the pod threshold level, and set modes and clocks.
- Trigger is available when an analyzer is set to State or Timing. Use Trigger to specify a trigger sequence which will filter the raw information into the measurement you want to see.
- Listing is available when an analyzer is set to State or Timing. Use Listing to view your measurement as a list of states. Using an inverse assembler, a state analyzer can display the measurement as though it were assembly code.
- Compare is available only when an analyzer is set to State. Use Compare to compare two listings and quickly scroll to the sections where they differ.



- Mixed Display always appears in the menu list when an analyzer is set to State or Timing, but it requires a State analyzer with time tags enabled.
- Waveform is available when an analyzer is set to State or Timing. Use Waveform to view the data as logic levels on discrete lines.
- Chart is available only when an analyzer is set to State. Use Chart to view your measurement as a graph of states versus time.
- SPA is available only when an analyzer is set to SPA. Use SPA to gather and view overall statistics about your system performance.

See Also

Chapter 8, "Reference," for details on the State and Timing menus and Chapter 9, "System Performance Analysis (SPA) Software," for information on the SPA menu.

"Using the Analyzer Menus" in this chapter for how to use the menus.

To access the Pattern Generator menus

The Pattern Generator menus let you configure the pattern generator, build test vector files, and use and create user macros.

1. **Select the mode field.**

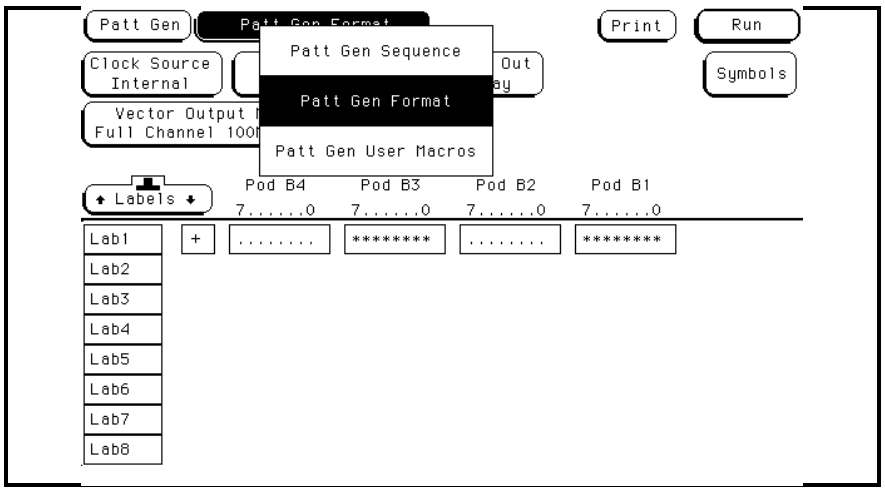
   A pop-up menu appears with the choices System, Analyzer, and Patt Gen. (If you have installed any optional software, there may be other choices as well.

2. **Select Patt Gen.**

3. **Select the menu field.**

   The menus for the pattern generator.

   - Patt Gen Sequence menu is used to build test vector files. There are two sequences: an initialization sequence and a main sequence.
   - Patt Gen Format menu is used to configure the pattern generator with a clock source and parameters, to generate a symbol table, to select its output mode, to assign which vector output channels are used, and to group and label the vector output channels.
   - Pat Gen User Macros menu is used to create new macros and to edit existing macros.



Using the Analyzer Menus

The following examples show how to use some of the Analyzer menus to configure the logic analyzer for measurements. These examples assume that you have already determined which signals are of interest, and have connected the logic analyzer to the target system. Some of the examples use data from a Motorola 68360 target system, acquired with an HP E2456A Preprocessor Interface.

To label channel groups

Hewlett-Packard logic analyzers give you the ability to separate or group data channels and label the groups with a name that is meaningful to your measurement. Labels also assist you in triggering only on states of interest.

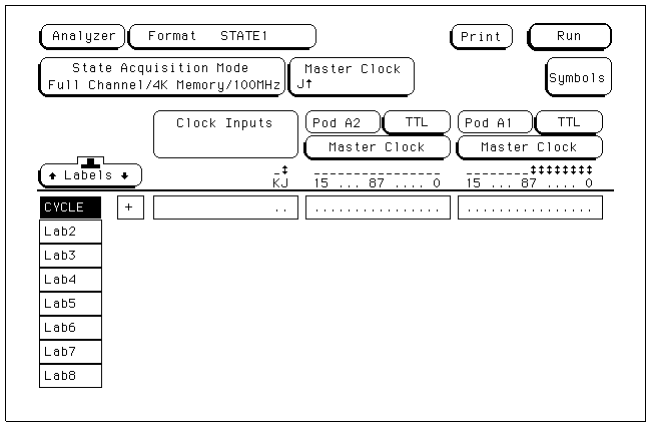
Labels can only be assigned in the Analyzer Format menu. Once assigned, the labels are available in all display menus, where they can be added to or deleted from the display. Use labels when you want to group data channels by function with a name that has meaning to that function.

The default label names are Lab1 through Lab126. However, you can modify a name to any six-character string. If you are using an HP preprocessor interface, the configuration file has predefined labels for your specific processor.

To create or modify a label and assign channel groups, use the following procedure.

1. **Press the Format key to go to the Format menu.**
2. **Select a label under the Labels heading. In the pop-up menu, select Modify Label.**
3. **Use the front panel to enter a name for the label and press Done.**

   In this example, the label is called CYCLE.



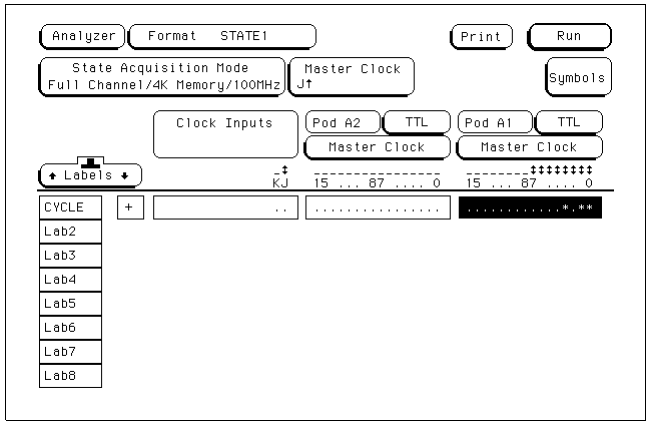
4 Select the pod containing the channels for the label. Use the knob or the arrow keys to position the selector over a channel you want to change.

An asterisk indicates the channel is selected; a dot indicates the channel is not part of the current group.

5 Toggle the channel's group status by pressing Select.

The indicator changes and the selector moves to the next channel.

In this example, the channels 3, 1, and 0 (Pod A1) are assigned to label CYCLE



To create a symbol

Symbols are alphanumeric mnemonics that represent specific data patterns or ranges. When you define a symbol and set the the base type to Symbol in the Listing menu, the symbol is displayed in the data listing where the bit pattern would normally be displayed. The symbols also appear in the Waveform menu when you view a label in bus form. Symbols allow you to quickly identify data of interest.

To create a symbol, use the following procedure.

1. **In the Analyzer Format menu, select Symbols.**

   The symbol table menu appears. The symbol table is where all user symbols are created and maintained. If you get a message, "No labels specified," check that you have at least one label turned on with channels assigned to it.

2. **In the Symbol menu, select the Label field. In the pop-up menu, select the label that contains the channel groups you want.**

   When you open the symbol table menu, the Label field displays the name of the first active label.

   If the label you want does not appear in the pop-up menu, the label is probably off. Return to the Format menu, select the label you want, and select Turn Label On. Another possibility is that the label is on the other analyzer. The two analyzers manage resources separately.

3. **Select the Base field. In the pop-up menu, select the base for the pattern.**

   In this example, binary is used because CYCLE only contains three channels.

4. **Select the field below Symbol. Select Add a Symbol, type in the symbol name, then press Done.**

5 If additional Symbols are needed, repeat step 4 until you have added all symbols.

   In this example, three symbols are added: MEM RD, MEM WR, and DATA RD.

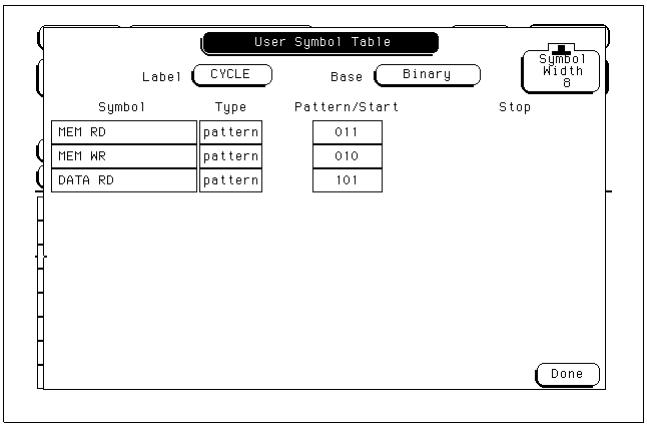
6 Toggle the Type field to "range" or "pattern".

   When Type is range, a third field appears under the Stop column. To fully specify a range, you need to enter a value for it, too.

7 Select the Pattern/Start field and use the keypad to enter an appropriate value in the selected base. Use X for "don't care."

8 When the pattern is specified, press Done. If you created additional Symbols, repeat steps 6 and 7 until all symbols are specified.

9 To close the symbol table menu, select Done.



Symbol table Menu Showing Three Symbols

You can also download symbol tables created by your programming environment using HP E2450A Symbol Utility. The Symbol Utility is shipped with the HP 1660CP-series logic analyzers.

See Also

HP E2450A Symbol Utility User's Guide for more information on the Symbol Utility.

To examine an analyzer waveform

The Analyzer Waveform menu lets you view state or timing data in a format similar to an oscilloscope display. The horizontal axis represents states (in state mode) or time (in timing mode) and the vertical axis represents logic highs and lows.

1. **In Analyzer mode, press the Run key to acquire data.**

   In any mode other than Analyzer, pressing the Run key has no effect. The menus which ignore Run lack the Run field onscreen. In Analyzer mode with Run available, the menu changes to a display menu.

2. **Go to the Analyzer Waveform menu.**

3. **To adjust the horizontal axis (sec/Div or states/Div), use the knob.**

   If nothing happens when you turn the knob, make sure the Div field has a roll indicator above it, as in the figures on the next page. When you first enter the Waveform menu, the knob adjusts the horizontal axis but if you select another rollable field, the knob will control that field instead.

4. **To adjust the display relative to the trigger, select the Delay field and enter a value or use the knob.**

   The portion of memory being displayed is indicated by a white bar along the bottom of the display area. The position of the trigger in memory is indicated by a white dot on the same line. When the bar includes the dot, then the trigger is visible on the display as indicated by a vertical line with a "t" underneath.

5. **To scroll through waveforms, select the large rectangle below the Div field and use the knob.**

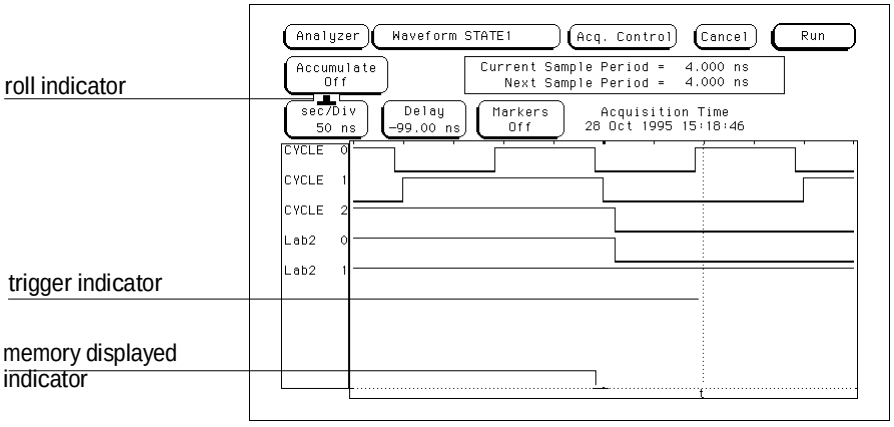
   The roll indicator appears at the top of the rectangle and the name of the first waveform is highlighted. The highlight moves as you turn the knob.

6. **To insert waveforms, select the large rectangle under the Div field. In the pop-up, select Insert, and then select the labels and channels.**

   The Sequential field inserts all the channels of the label as individual waveforms; the Bus field groups the waveforms; the Bit N field inserts just the Nth bit. Waveforms are inserted after the currently highlighted one.

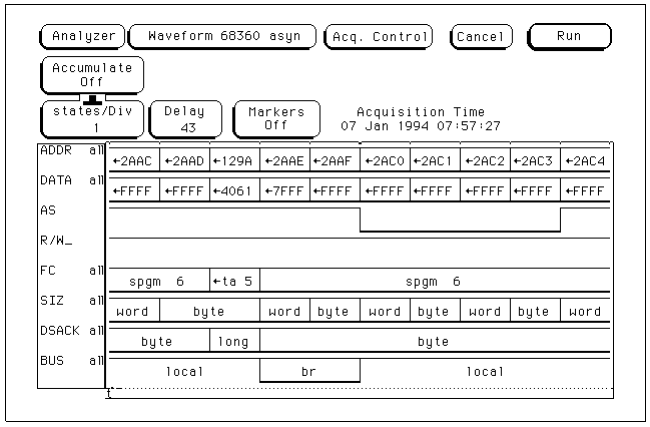
7 To take measurements, select the Markers field and choose the appropriate marker type.

The markers available depend on the type of analyzer and whether or not tagging is enabled. Use markers to locate patterns quickly.



Example

The following example shows a state waveform from the Hewlett-Packard preprocessor interface for the Motorola 68360. Notice how the bus waveforms insert symbols or state data.



To examine an analyzer listing

The Analyzer Listing menu displays state or timing data as patterns (states). The Listing menu uses any of several formats to display the data such as binary, ASCII, or symbols. If you are using an inverse assembler and select Invasm, the data is displayed in mnemonics that closely resemble the microprocessor source code.

See Also

"The Inverse Assembler" at the end of this chapter for additional information on using an inverse assembler.

1. **In Analyzer mode, press the Run key to acquire data.**

   In any mode other than Analyzer, pressing the Run key has no effect. The menus which ignore Run lack the Run field onscreen. In Analyzer mode with Run available, the menu changes to a display menu.

2. **Go to the Analyzer Listing menu.**

   All labels defined in the Analyzer Format menu appear in the listing. If there are more labels than will fit on the screen, the Label/Base field is shaded like a normal field.

3. **To scroll the labels, select the Label/Base field and use the knob or press the blue shift key and a page key.**

   If the Label/Base field is selectable, the roll indicator appears over the field as in the example. To move the labels one full screen at a time, press Shift and a Page key.

4. **To scroll the data, use the Page keys or select the data roll field and use the knob.**

   If you select the data roll field, the roll indicator moves to it. No matter which field is currently controlled by the knob, however, the Page keys page the data up or down.

   The numbers in the data roll column indicate how many samples the data is from the trigger. Negative numbers occurred before the trigger and positive numbers occurred after.

5. **If the labels have symbols associated with them, set the base to Symbol.**

   The symbols you defined appear in the listing.

6 To insert a label, select one of the label fields, then select Insert from the pop-up and the label you want to insert.

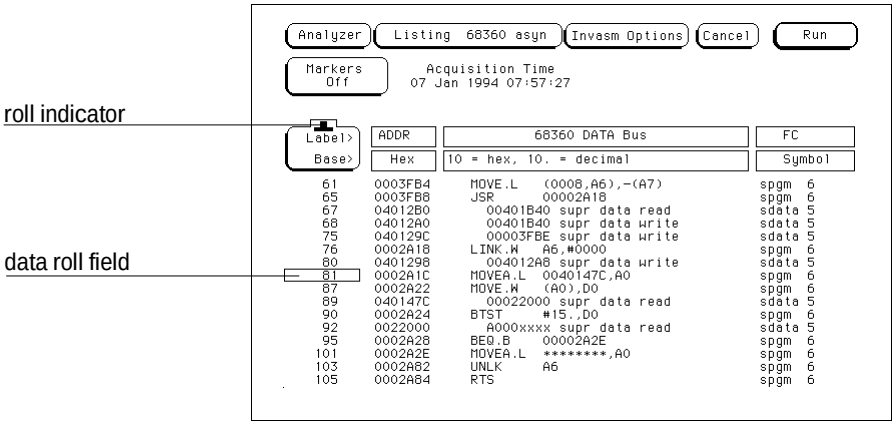
The last label cannot be deleted, so there is always at least one label. You can insert the same label multiple times and display it in different bases.

7 To take measurements, select the Markers field and choose the appropriate marker type.

The markers available depend on the type of analyzer and whether or not tagging is enabled. Use markers to locate states quickly.

Example

The following illustration shows a listing from the Hewlett-Packard preprocessor interface for the Motorola 68360. The ADDR label has the base set to Hex to conserve space on the display. The DATA label has the base set to Invasm for inverse assembly. The FC label has the base set to Symbol. Additional labels are located to the right of FC, and can be viewed by highlighting and selecting Label, then using the knob to scroll the display horizontally.



To compare two listings

The Compare menu allows you to take two state analyzer acquisitions and compare them to find the differences. You can use this function to quickly find all the effects after changing the target system or to quickly compare the results of quality tests with results from a working system.

1. **In Analyzer mode, press the Run key to acquire data.**

   In any mode other than Analyzer, pressing the Run key has no effect. The menus which ignore Run lack the Run field onscreen. In Analyzer mode with Run available, the menu changes to a display menu.

2. **Go to the Analyzer Compare menu, select Copy Listing to Reference, and then select Execute.**

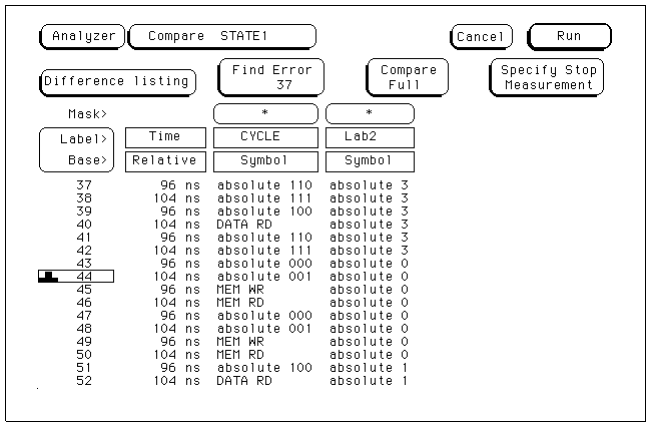
   The Compare menu initially is empty, but when you select Execute the data appears.

3. **Set up the other test that you want to compare to the first.**

   This can be a change to the hardware, or a different system. Do not change the trigger, however, or all the states will be different.

4. **Run the test again, then select the Reference listing field to toggle to Difference listing.**

   The Difference listing is displayed on the next page.



The Difference listing displays the states that are identical in dark typeface, and the states that are different in light typeface (indistinguishable in the above illustration). The light typeface shows the data from the compare file that is different from the data in the reference file.

5 Select the Find Error field and use the knob to scroll through the errors.

The display jumps past all states that are identical, and shows the number of errors through the current state in the Find Error field. In the above illustration, there are 37 errors through state 44 of the listing.

The Inverse Assembler

When the analyzer captures a trace, it captures binary information. The analyzer can then present this information in symbol, binary, octal, decimal, hexadecimal, or ASCII. Or, if given information about the meaning of the data captured, the analyzer can inverse assemble the trace. The inverse assembler makes the trace list more readable by presenting the trace results in terms of processor opcodes and data transactions.

To use an inverse assembler

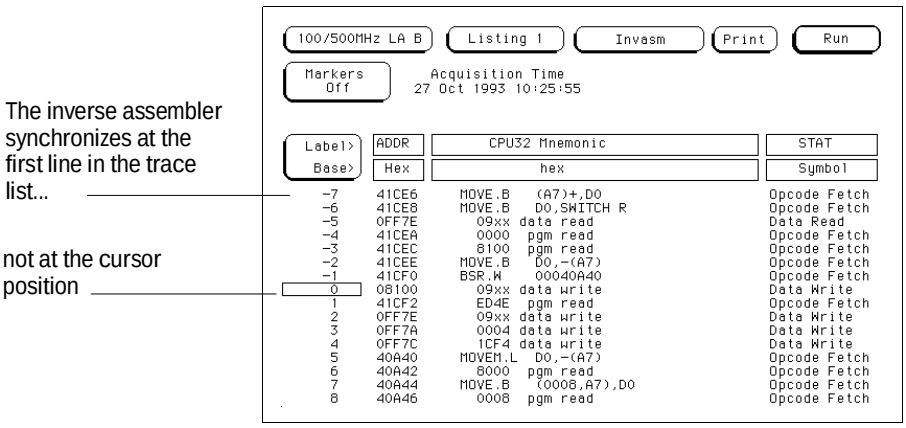
Most preprocessors include an inverse assembler in their software. Loading the configuration file for the preprocessor sets up the logic analyzer to provide certain types of information for the inverse assembler. This section is provided in case you ever have to set up an analyzer for inverse assembly yourself.

The inverse assembly software needs at least these five pieces of information:

- Address bus. The inverse assembler expects to see the label ADDR, with bits ordered in a particular sequence.
- Data bus. The inverse assembler expects to see the label DATA, with bits ordered in a particular sequence.
- Status. The inverse assembler expects to see the label STAT, with bits ordered in a particular sequence.
- Start state for disassembly. This is the first displayed state in the trace list, *not* the cursor position. See the figure on the next page.
- Tables indicating the meaning of particular status and data combinations.

The particular sequences that each label requires depends on the type of chip the inverse assembler was designed for. Because of this, inverse assemblers cannot generally be transferred between platforms.

To run the inverse assembler, you must be sure the labels are spelled correctly as shown here, or as directed in your inverse assembler documentation. Even a minor difference such as not capitalizing each letter will cause the inverse assembler to not work.



Inverse Assembly Synchronization

When you press the Invasm key to begin inverse assembly of a trace, the inverse assembler begins with the first displayed state in the trace list. This is called *synchronization.* It looks at the status bits (STAT) and determines the type of processor operation, which is then displayed under the STAT label. If the operation is an opcode fetch, the inverse assembler uses the information on the data bus to look up the corresponding opcode in a table, which is displayed under the DATA label. If the operation is a data transfer, the data and corresponding operation are displayed under the DATA label. This continues for all subsequent states in the trace list.

If you roll the trace list to a new position and press Invasm again, the inverse assembler repeats the above process. However, it does not work backward in the trace list from the starting position. This may cause differences in the trace list above and below the point where you synchronized inverse assembly. The best way to ensure correct inverse assembly is to synchronize using the first state you know to be the first byte of an opcode fetch.

See Also

The *Preprocessor User's Guide* for more information on controlling inverse assembly. If you have problems using the inverse assembler, see "Troubleshooting" in chapter 11.

Using the Trigger Menu

Using the Trigger Menu

To use the logic analyzer efficiently, you need to be able to set up your own triggers. This chapter provides examples of triggering. Those examples assume you already know where to find fields in the trigger menu.

This chapter shows you how to:

- Specify a basic trigger
- Change a trigger sequence
- Set up time correlation between analyzers
- Arm from another instrument, or arm another instrument
- Manage memory

Specifying a Basic Trigger

The default analyzer triggers are

```
While storing "anystate" TRIGGER on "a" 1 time
```

```
Store "anystate"
```

for state analyzers and

```
TRIGGER on "a" > 8 ns
```

for timing analyzers. If you want to simply record data, these will get you started. They can quickly be tailored by specifying a particular pattern to look for instead of the general case.

Customizing a trigger generally requires these steps:

- Assign terms to both analyzers.
- Define the terms.
- Change the trigger to use the new terms.

To assign terms to an analyzer

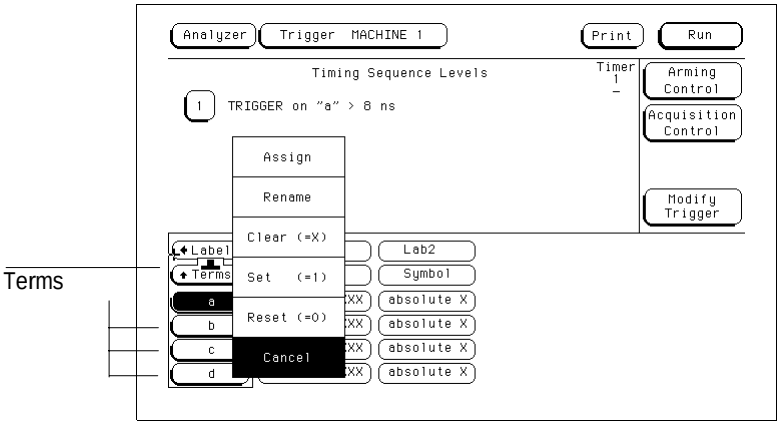
When you turn the logic analyzer on, Analyzer 1 is named Machine 1 and Analyzer 2 is off. Because trigger terms can only be used by one analyzer at a time, all the terms are assigned to Analyzer 1. If you plan to use both analyzers in your measurement, you need to assign some of the terms to Analyzer 2.

1 Go to the Trigger Machine 1 menu.

If you have renamed Machine 1 in the Analyzer Configuration menu, the name you changed it to will appear in the menu instead of Machine 1.

2 Select a term.

The terms are the fields below the roll field "Terms". See the figure below.



3 Select Assign from the list that appears.

The Resource Term Assignment menu appears. It is divided into two sections, one for each analyzer. All terms are listed.

4 To change a term assignment, select the term field.

The term fields toggle from one section to the other. You can get all your terms assigned at once, or just change a few to meet immediate needs.

5 To exit the term assignment menu, select Done.

To define a term

Both default triggers trigger on term "a". If you only need to look for the occurrence of a certain state, such as a write to protected memory, then you only need to define term "a" to make the measurement you want.

1. **In the Trigger menu, select the field at the intersection of the term and the label whose value you want to trigger on.**

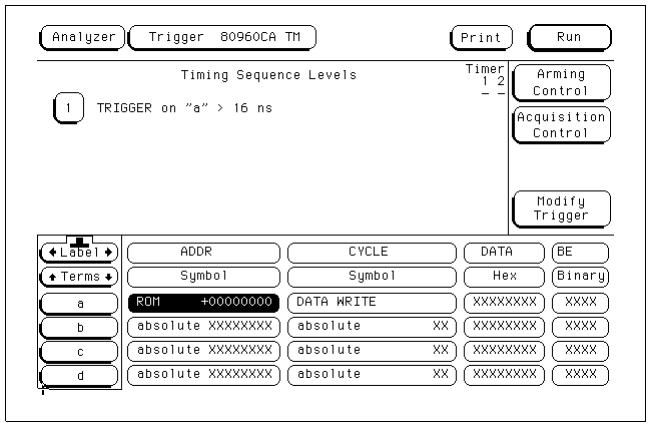
   You set labels in the Analyzer Format menu. If the channels you want to monitor are not attached to a label, they will not appear in the trigger menu.

2. **Enter the value or pattern you want to trigger on.**

   If the label's base is Symbol, a pop-up menu appears offering a choice of symbols. For other bases, use the keypad. An "X" stands for "don't care".

   If there are two conditions that need to be present at the same time, for example a protected address on the address bus and a write on the read/write line, define both values on the same term. See the figure below.

3. **Press Done.**



Term "a" Defined as a Data Write to Read-Only Memory

To change the trigger specification

Most triggers use terms other than "a." Even a simple trigger might use additional terms to set conditions on the actual trigger. To use these terms, you must include them in the trigger sequence specification.

1. **In the Trigger menu, select the number beside the specific level you want to modify.**

   A Sequence Level menu pops up. It shows the current specification for that trigger level.

2. **Select the field you want to change.**

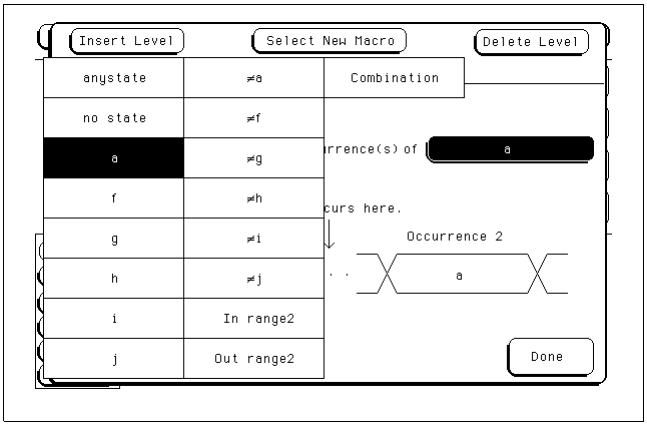
   In the top row of the pop-up are three action fields: Insert Level, Select New Macro, and Delete Level. The next section goes into detail on them. The fields after "While storing", "TRIGGER on", and "Else on" are completed with trigger terms. Selecting these fields pops up a menu of terms.

3. **Select the term you want to use from the pop-up, or enter a new value, as appropriate to the field.**

   Selecting "Combination" pops up a menu to define a term combination. The combination mechanism is discussed in "Resource terms" in Chapter 8 and "The Trigger Sequence" in Chapter 10.

   If you have renamed a term, that name is automatically used everywhere the term would appear.

4. **Select Done until you are back at the Trigger menu.**



Term Selection Pop-up Menu

Changing the Trigger Sequence

Most measurements require more complicated triggers to better filter information. From the basic trigger, you can:

- Add sequence levels
- Change macros

Your logic analyzer provides a macro library to make setting up the trigger easier. There are 12 state macros and 13 timing macros. Most macros take more than one level internally to implement, and can be broken down into their separate levels. Once broken down, the levels can be used to design your own trigger sequences.

To add sequence levels

You can add sequence levels anywhere except after the final one.

1. **In the Trigger menu, select the number beside the sequence level just after where you want to insert.**

   For example, if you want to insert a sequence level between levels 1 and 2, you would select level 2. To insert levels at the beginning, select level 1.

   A Sequence Level pop-up appears. Its exact contents depend on the analyzer configuration and the level specification. However, all Sequence Level pop-ups have an Insert Level field in the upper left corner.

2. **Select Insert Level.**

   Another pop-up offers the choices of Cancel, Before, or After. If the level you started from was the last level, After will not appear.

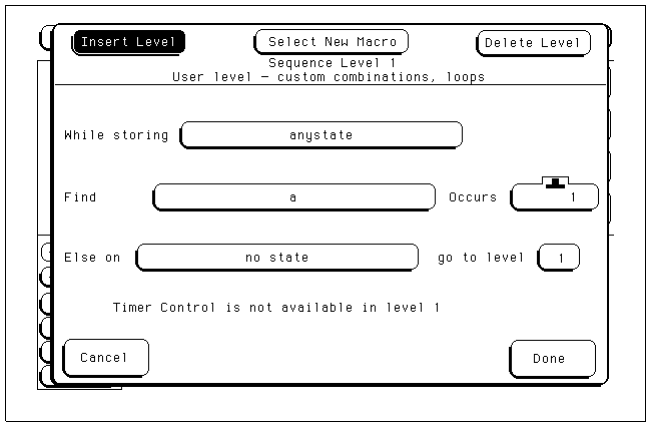
3. **Select Before.**

   The Trigger Macro pop-up replaces the Sequence Level pop-up. The macros available depend on whether the analyzer is configured as state or timing.

4. **Use the knob to highlight a macro, and select Done.**

   A new Sequence level pop-up appears. Its contents reflect the macro you just selected. The figure below shows a user macro for a state analyzer.

5. **Fill in the fields and select Done.**



Sequence Level Pop-up Menu

To change macros

You do not need to add and delete levels just to change a level's macro. This can be done from within the Sequence Level pop-up.

1. **From the Trigger menu, select the sequence level number of the sequence level you want to modify.**

   A Sequence Level pop-up appears. Its contents reflect the current macro.

2. **Select Select New Macro.**

   The Trigger Macro pop-up replaces the Sequence Level pop-up. The macros available depend on whether the analyzer is configured as state or timing.

3. **Use the knob to highlight the macro you want, and select Done.**

   A new Sequence Level pop-up appears. Its contents reflect the macro you just selected. The wording of this screen is very similar to the macro description, and the line drawing demonstrates what the macro is measuring.

4. **Select the appropriate assignment fields and insert the desired pre-defined terms, numeric values, and other parameter fields required by the macro. Select Done.**

   For state analyzers, a final "go to trigger" level is automatically placed at the end of the trigger specification for you. This level must always be a user level. Although you can change its fields, you cannot change the macro. Timing analyzers do not have this restriction.

See Also

"Timing Trigger Macro Library" and "State Trigger Macro Library" in The Analyzer Trigger Menu in Chapter 8 for a complete listing of macros.

Setting Up Time Correlation between Analyzers

There are two possible combinations of analyzers: state and state, and state and timing. Timing and timing is not possible because the Analyzer Configuration menu only permits one analyzer at a time to be configured as a timing analyzer. For either combination, time correlation is necessary for interleaving and mixed display.

Time correlation is useful when you want to store different sorts of data for each trace, but see how they are related. For instance, you could set up a timing and a correlated state analyzer and see if setup and hold times are being met. Or, you could set up two state analyzers and have one watch normal program execution and the other watch the control and status lines.

Time correlation requires that state analyzers store time tags. You set the state analyzer to store time tags by turning on Count Time in the Analyzer Trigger menu. The timing analyzer already stores time tags when it samples data.

See Also

"Special displays" in Chapter 6 for more information on interleaving and mixed display.

To set up time correlation between two state analyzers

To correlate the data between two state analyzers, both must have Count Time turned on in their Trigger menus. Although both have Count State available, it is not possible to correlate data based on states even when they are identically defined.

1. In the Analyzer Trigger menu, select Count.

   Count may be Count Off, Count Time, or Count States. Selecting the field causes a pop-up to appear.

2. Select the field after Count: and select Time.

   A warning may appear about reduced memory. It will not prevent you from changing Count to Count Time.

3. Select Done.

4. Repeat steps 1 through 3 for the other state analyzer.

   Now when you acquire data you will be able to interleave the listings.

To set up time correlation between a timing and a state analyzer

To set up time correlation between a timing and a state analyzer, only the state analyzer needs to have Count Time turned on. The timing analyzer automatically keeps track of time.

1. In the state Analyzer Trigger menu, select Count.

   Count may be Count Off, Count Time, or Count States. Selecting the field causes a pop-up to appear.

2. Select the field after Count: and select Time.

   A warning may appear about reduced memory. It will not prevent you from changing Count to Count Time.

3. Select Done.

   Now when you acquire data you will be able to set up a mixed display.

Arming and Additional Instruments

Occasionally you may need to start the analyzer acquiring data when another instrument detects a problem. Or, you may want to have the analyzer itself arm another measuring tool. This is accomplished from the Arming Control field of the Analyzer Trigger menu.

To arm another instrument

1. **Attach a BNC cable from the External Trigger Output port on the back of the logic analyzer to the instrument you want to trigger.**

   The External Trigger Output port is also referred to as "Port Out." It uses standard TTL logic signal levels, and will generate a rising edge when trigger conditions are met.

2. **In the Analyzer Trigger menu, select Arming Control.**

   Arming Control is below the Run button.

3. **Select the field near Arm Out, and choose PORT OUT.**

4. **If you are using both analyzers, set the Arm Out Sent From field in the upper right corner.**

   This field does not appear if only one analyzer is configured.

   The selected analyzer will send the arm signal when it finds its trigger.

5. **Select Done.**

   When you make a measurement, the analyzer will send an arm signal through the External Trigger Output when the analyzer finds its trigger.

To receive an arm signal from another instrument

When you set the analyzer to wait for an arm signal, it does not react to data that would normally trigger it until after it has received the arm signal. The arm signal can be sent to any of the Trigger Sequence levels, but will go to level 1 unless you change it. Setting up the analyzer to receive an arm signal is more efficient when the sequence levels are already in place.

1 Connect a BNC cable from the instrument which will be sending the signal to the External Trigger Input port on the back of the logic analyzer.

CAUTION Do not exceed 5.5 volts on the External Trigger Input.

The External Trigger Input port is also referred to as "Port In." It uses standard TTL logic signal levels, and expects a rising edge as input.

2 In the Analyzer Trigger menu, select Arming Control.

Arming Control is below the Run button. .

3 Select the leftmost field, and choose PORT IN.

The field is unlabeled and shows either Run or PORT IN. It has arrows going from it to the analyzer(s).

4 To change the default settings, select the analyzer field.

A small pop-up menu appears. To change which device the analyzer is receiving its arm signal from, select the Run from field. To change which sequence level is waiting for the arm signal, select the Arm sequence level field.

5 Select Done until you are back at the Trigger menu.

Sometimes you will need every last bit of memory you can get on the logic analyzer. There are three simple ways to maximize memory when specifying your trigger:

- Selectively store branch conditions (State only)
- Place the trigger relative to memory
- Set the sampling rates (Timing only)

To selectively store branch conditions (State only)

Besides setting up your trigger levels to store anystate, no state, or some subset of states, you can also choose whether or not to store branch conditions. Branch conditions are always stored by default, and can make tracing the analyzer's path through a complicated trigger easier. If you really need the extra memory, however, it is possible to not store the branch conditions.

You cannot set the analyzer to store only some branches in a trigger sequence specification.

1 In the Analyzer Trigger menu, select Acquisition Control.

The Acquisition Control menu pops up. If the acquisition mode is set to Automatic, the menu contains a single field and an explanation. If Acquisition has been customized, it has 3 fields and a picture showing where the trigger is currently placed in memory.

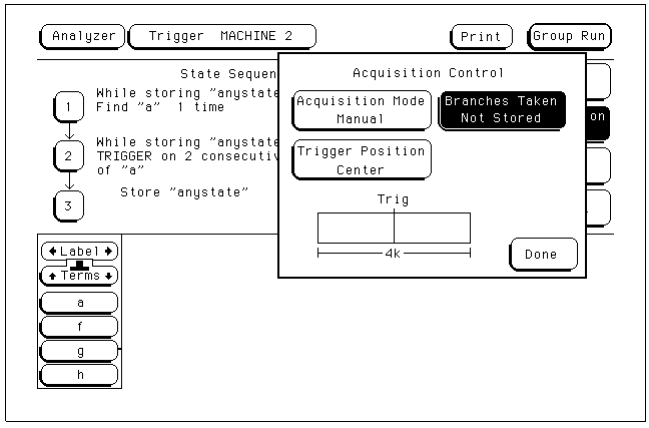
2 If the mode is Automatic, select the field and toggle it to Manual.

The menu now shows three fields and a picture.

3 Select the Branches Taken Stored field.

It toggles to Branches Taken Not Stored.

4 Select Done.



Acquisition Control Menu with Branches Field Highlighted

To place the trigger in memory

In Automatic Acquisition Mode, the exact location of the trigger depends on the trigger specification but usually falls around the center. You can manually place it at the beginning, end, or anywhere else.

1 In the Analyzer Trigger menu, select Acquisition Control.

The Acquisition Control menu pops up. If the acquisition mode is set to Automatic, the menu contains a single field and an explanation. If Acquisition has been customized, it has 3 or 4 fields and a picture showing where the trigger is currently placed in memory.

2 If the mode is Automatic, select the field to toggle it to Manual.

The menu now shows three fields and a picture.

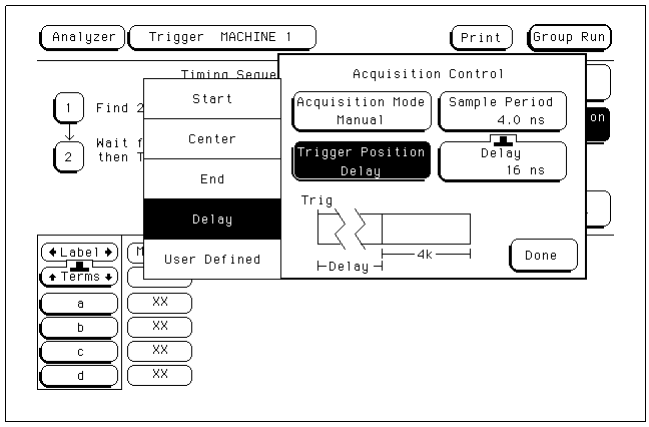
3 Select the Trigger Position field.

A list of choices appears, as shown in the timing trigger example below.

4 Select the appropriate entry for your needs.

Start, Center, and End place the trigger respectively at the beginning, middle, and end of the memory. Delay, available in timing analyzers only, causes the analyzer to not save any data before the time delay has elapsed. User Defined calls up a fourth field where you specify exactly where you want the trigger.

5 Select Done.



Acquisition Control Menu with Trigger Position Pop-up for a Timing Analyzer

To set the sampling rates (Timing only)

A timing analyzer samples the data based on its own internal clock. A short sample period provides more detail about the device under test; a long sample period allows more time before memory is full. However, if the sample period is too large, some information may be missed.

1. **In the Analyzer Trigger menu, select Acquisition Control.**

   The Acquisition Control menu pops up. If the acquisition mode is set to Automatic, the menu contains a single field and an explanation. If Acquisition has been customized, it has 3 or 4 fields and a picture showing where the trigger is currently placed in memory.

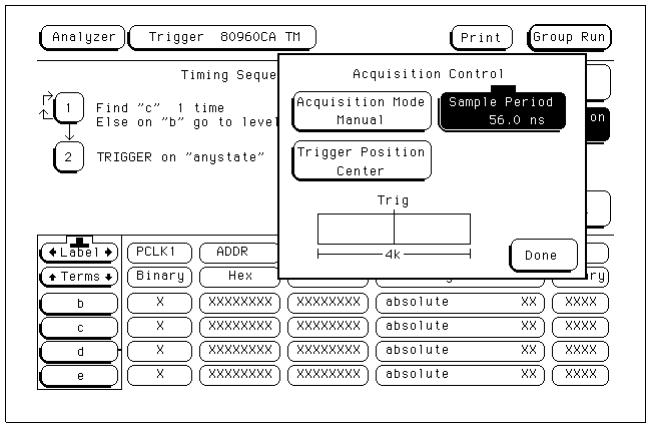
2. **If the mode is Automatic, select the field and toggle it to Manual.**

   The menu now shows three fields and a picture.

3. **Set the Sample Period field using the knob, or select it to use the keypad to enter the period.**

4. **Select Done.**

   Next time you take a measurement, the analyzer will sample at the rate you entered.



Acquisition Control Menu with Sample Period Selected

Using the Pattern Generator

Using the Pattern Generator

This chapter provides instructions for using the pattern generator to generate vectors and patterns for design and test environments. It also covers the pattern generator common menus, loading ASCII files, and the pattern generator probing system.

This chapter covers:

- Setting up the proper configurations
- Building test vectors and macros
- Pattern generator common menus
- Loading ASCII files
- Pattern generator probing system

Setting Up the Proper Configurations

This section discusses setting up the configuration attributes and parameters of the pattern generator.

If you are reloading existing configurations or downloading ASCII vector files, refer to the Load operation in the disk drive menus of the System.

To set up the configuration

1. **From the Format menu, set the Vector Output Mode to either full- or half-channel.**

   Make this selection first because clock frequencies and available channels are affected.

   In half-channel mode, only pods 1 and 3 are used.

2. **Set the Clock Source to either internal or external.**

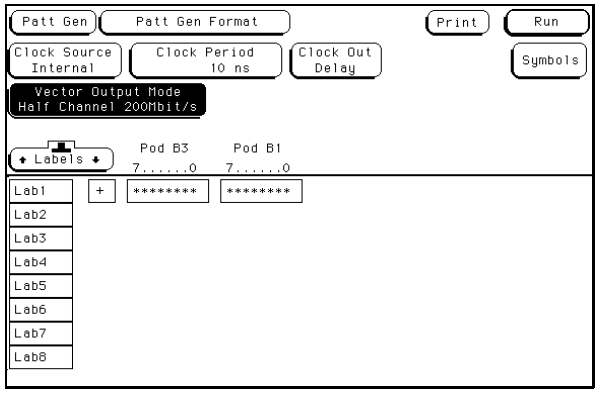
   An external clock is used when you need a clock frequency that is not available internally, or if you need to drive the pattern generator timing with an external reference.

3 Set the Clock Period for an internal clock or the Clock Frequency for an external clock.

The external clock frequency information is required to select the appropriate operating mode. Operating the pattern generator at an external clock frequency higher than selected will result in erroneous operation.

4 Set the Clock Out Delay if a delay is needed.

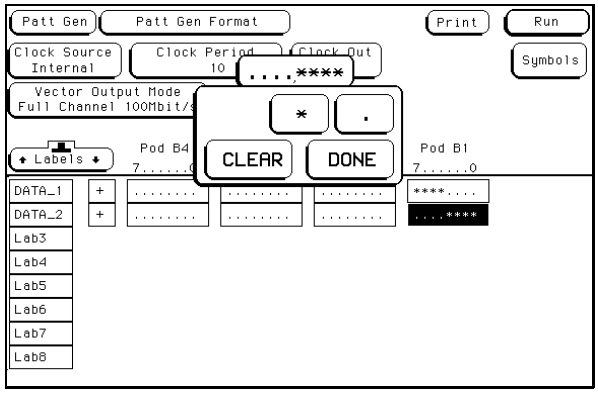
Setting a delay is useful when using the clock out edge as a read strobe. If you do not set the Clock Out Delay, the value is uncalibrated.



To build a label

When you build a label, you are grouping channels under a label name and mapping the selected channels to the probes on the associated pods. A label may contain a maximum of 32 channels, however, a single channel cannot be used under more than one label.

1 Select the label's channel assignment field.



2 Select the desired channels.

* (asterisk) = on

. (period) = off

Only the selected channels can output pattern generator signals.

3 Select Done.

Once the pattern generator is configured, you will want to build programs to use in your test system. You build programs in the Sequence menu. If you have small program segments that are built from frequently used vectors, they can be built in the User Macros Sequence menu.

Another way to build programs is to generate them on another system, then load them as ASCII files. For more information, refer to "Loading ASCII files" on page 5-36.

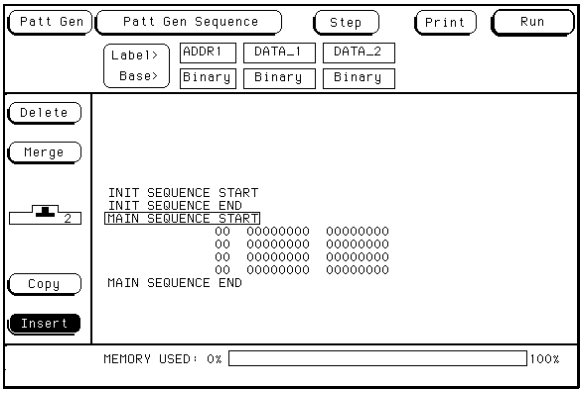
To build a main vector sequence

During a single run, the program vectors in the MAIN SEQUENCE are output to the system under test in an order of first vector to last vector. The data of the last vector is then held until run is selected again. During a repetitive run, the MAIN SEQUENCE loops until stop is selected.

1. From the Sequence menu, use the knob to highlight the first data row.
2. Select the Insert field once for each line of vectors you want inserted into the main sequence.

   These new lines of vectors provide fields to place data into for each label.
3. Select the data field, then type in a data value.

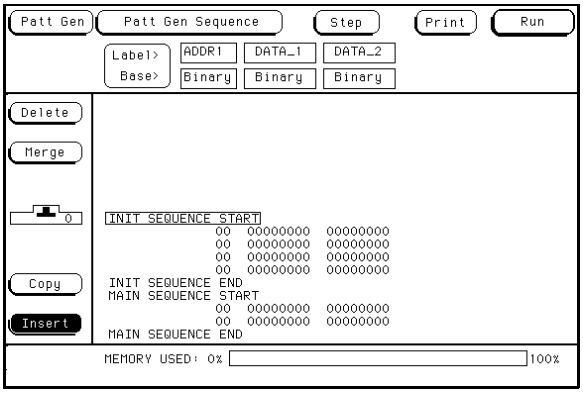
   If you will be adding data in many fields, use the Autoroll feature. Refer to "To use Autoroll" later in this chapter.



To build an initialization sequence

Use the INIT SEQUENCE to place the system under test into a known initialization state. Default start and end program vectors are marked INIT SEQUENCE START and INIT SEQUENCE END. During a repetitive run, the initialization sequence is only executed the first time the program is run. The main sequence then loops repetitively.

1 From the Sequence menu, use the knob to highlight INIT SEQUENCE START.



2 Select the Insert field once for each new line of vectors you want inserted into the initialization sequence.

These new lines of vectors provide fields to place data into for each label.

3 Select the data field, then type in a data value.

If you are adding data in many fields, use the Autoroll feature. Refer to "To use Autoroll" later in this chapter.

To edit a main or initialization sequence

1 Using the knob, highlight the vector you want to edit.

2 Select the data field you want to edit.

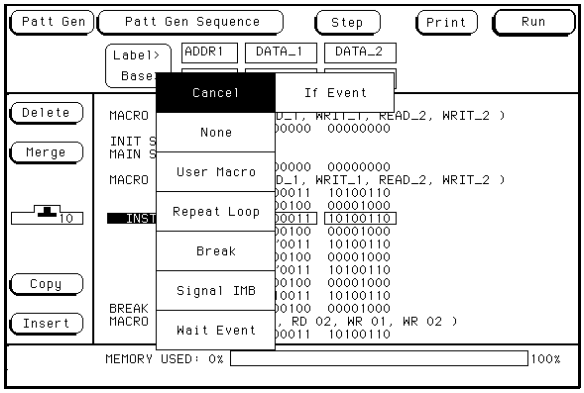
3 Select the new instruction or change the data value.

To include hardware instructions in a sequence

The following hardware instruction types are available:

- Break
- Signal IMB
- Wait Event
- If Event

1 Highlight the vector that you want to output as a hardware instruction.
2 Select the INST field of the highlighted vector.
3 Select the desired hardware instruction type.
4 If required, select any qualifying actions for the hardware instruction.



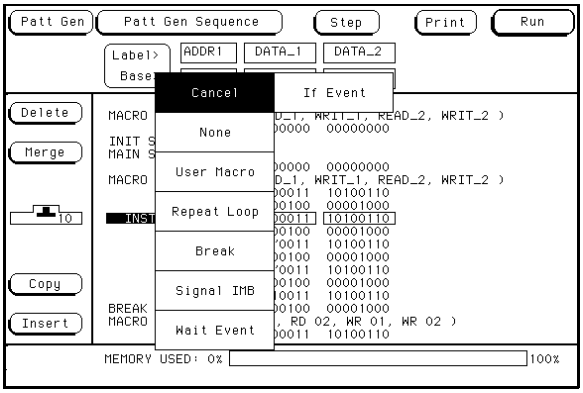
To include software instructions in a sequence

The following software instructions are available:

- User Macro
- Repeat Loop

If you are inserting a User Macro and have not yet built the macro, go to "To build a user macro" later in this chapter. Macros must be built before they can be inserted. To include these instructions in a sequence, use the following procedure.

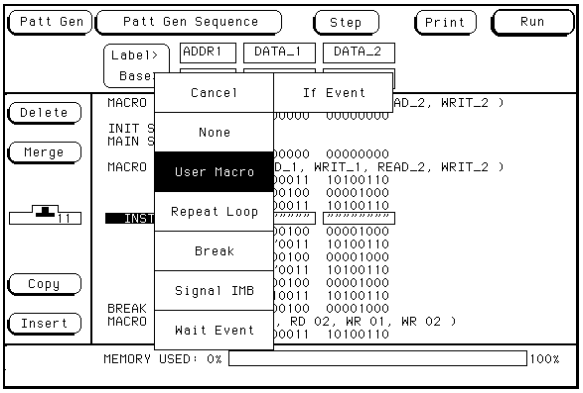
1. Highlight the vector that will be output at the time of the instruction.
2. Select the INST field.
3. Select the desired software instruction to insert.
4. If required, select any qualifying actions for the instruction.



To include a user macro in a sequence

If you have user macros, you can include them in the vector sequence using the following procedure. (If you have not yet built user macros, turn to "To build a user macro" to build needed macros.)

1. Insert a new vector where you want to place the user macro.
2. Highlight this new vector using the knob, then select the INST field.
3. Select the User Macro field.



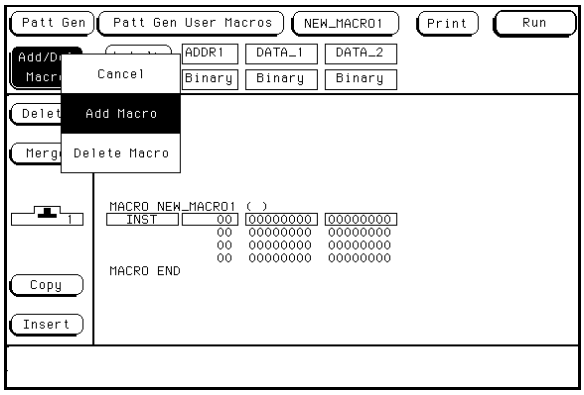
4. Select the user macro you want to insert from the list provided in the pop-up.

To build a user macro

Build macros for sequences of vectors you will want to use in multiple places. You can then insert these macros in INIT or MAIN sequences. Give each macro a name that will help you identify its function and make it easier to select from the list of macros you've built.

1. From the User Macros menu, select the Add/Del Macro field, then select ADD MACRO.
2. Select the MACRO field, then type the new macro name.
3. Add any desired parameters.

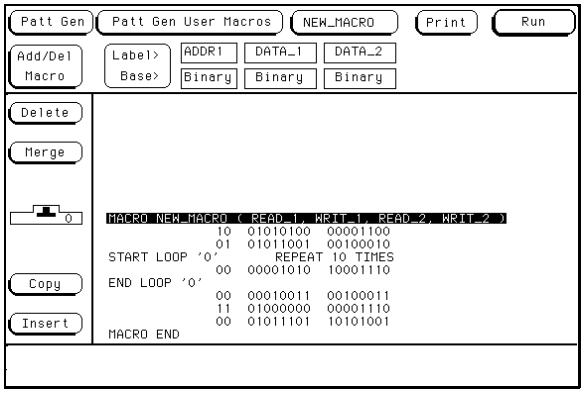
   Parameters are set when they are inserted into MAIN or INIT sequences. For more information on adding parameters, refer to "Adding parameters" found later in this chapter.
4. Select the Insert field to add as many vectors as needed into the macro.
5. Highlight the desired vector to modify.
6. Highlight a data field and insert the appropriate data.



To modify a macro name

If you rename a macro, the new macro name will be displayed in INIT and MAIN sequences where the macro has been used.

1. Select the macro to be renamed from the list of macros.
2. Highlight the first line of the macro, then select the field.
3. Modify the macro name, then select Done.



To edit a macro

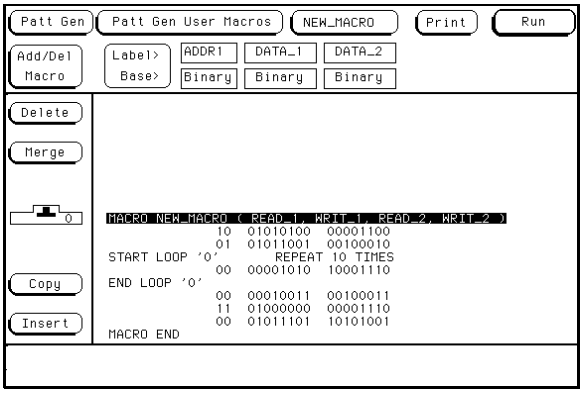
1. Highlight the vector you want to edit using the knob.
2. Select the field you want to edit.
3. Select the new instruction or change the data values using the pop-up or front panel.

To add, delete, or rename parameters

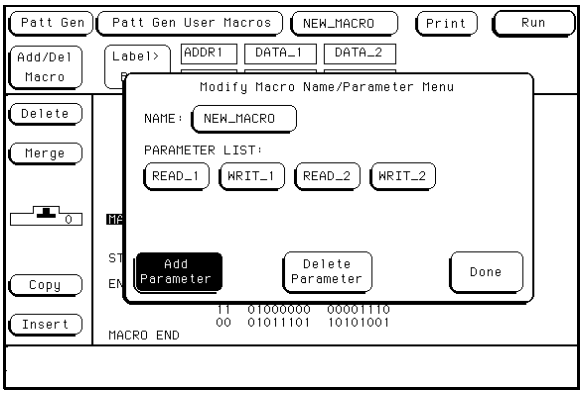
Parameters are set when they are inserted into MAIN or INIT sequences. The changes you make in the parameter list will appear every place in the INIT or MAIN sequences in which you have used that macro.

1 From the User Macros menu, select a macro from the list of macros.

2 Highlight the first line of the macro, then select the field.



3 To add a parameter, select Add Parameter, then select the new parameter field that appears and rename the parameter.

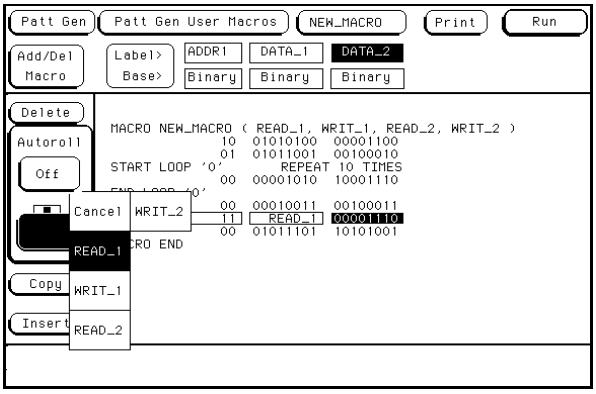


4 To delete a parameter from the parameter list, select a parameter name, then select Delete Parameter.

To place parameters in a vector

Once parameters are added to the parameter list, you insert them into data fields in macro vectors.

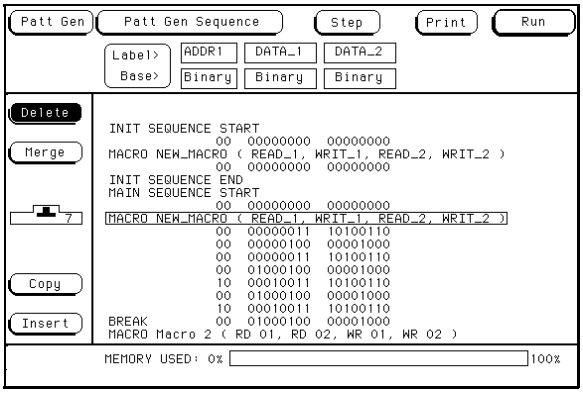
1. From the User Macro menu, select the desired data field in a vector.
2. Select the Set Param field. From the parameter list that appears, select the desired parameter to insert.



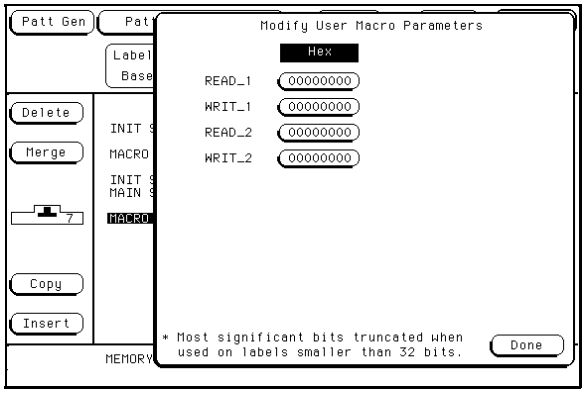
To enter or modify parameters

Each time you include a macro in an initialization or main sequence, you should enter the parameters for that particular instance. To enter or modify macro parameters, use the following procedure.

1 From the Sequence menu, highlight the line which contains the macro name, then select the field.



2 Enter or modify the parameter in the pop-up menu.



3 Select Done.

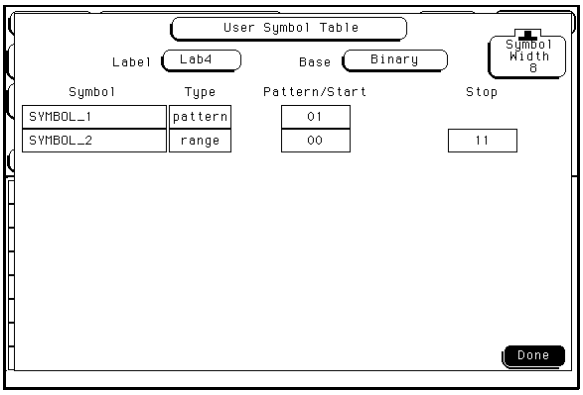
To build a User Symbol Table

You may want to build a symbol table to make inserting values into your program easier. You can name a symbol for one value in a label and insert that symbol into your vector sequence where you need it.

1. From the Format menu, select the Symbols field at the right of the menu.
2. Set the desired Label, Base, and Symbol Width.

   Symbols are specific for a given label. Symbol width determines the width of the symbolic name displayed in the Sequence menu.
3. Select the Symbol field, then enter a name for the symbol.
4. Select the desired symbol Type, then enter the Pattern/Start and Stop values.

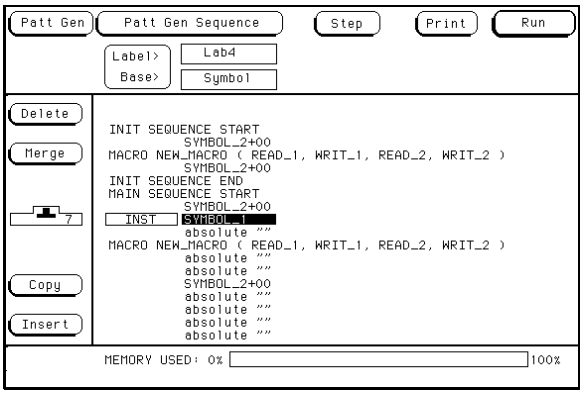
   The type is either a pattern or a range. A range provides a symbolic method for defining values within a specified range.
5. If you want to add more symbols, select the Symbol field Then select Add a Symbol, and repeat steps 2 through 4.
6. Select Done.



To include symbols in a sequence

Symbols must be created before they become available for insertion. See the task on the preceding page for more information.

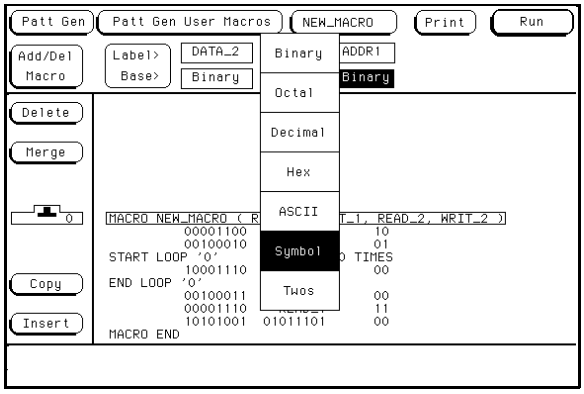
1. From the Sequence menu, select the Base field under the desired label where you want a symbol used.
2. From the Base selection list, select Symbol.
3. Highlight the desired vector, then select the data field.
4. Select the desired predefined symbol name.



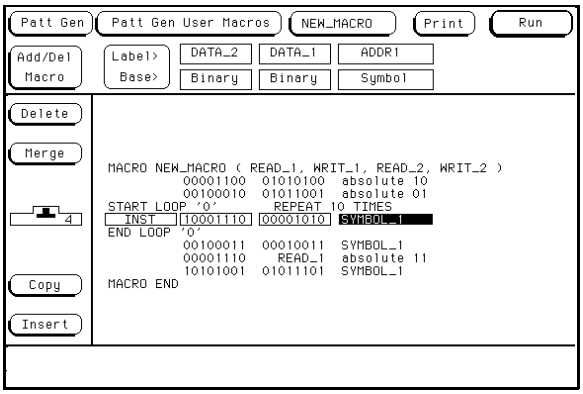
To include symbols in a macro

In the Format menu, you assign symbols to data under a given label. Once assigned, these symbols can be included under the same label in a macro.

1 From the User Macros menu, select the label Base field for any label that has pre-assigned symbols. Then, select Symbol from the Base selection list.



2 Highlight any vector in the macro. Then, select the data field under the label that has the pre-assigned symbol.

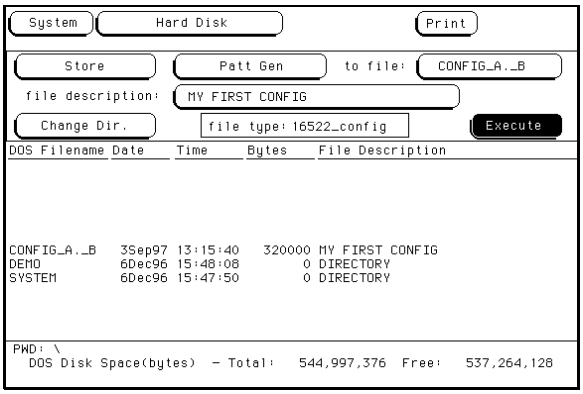


3 Select the symbol name you want displayed.

To store a configuration

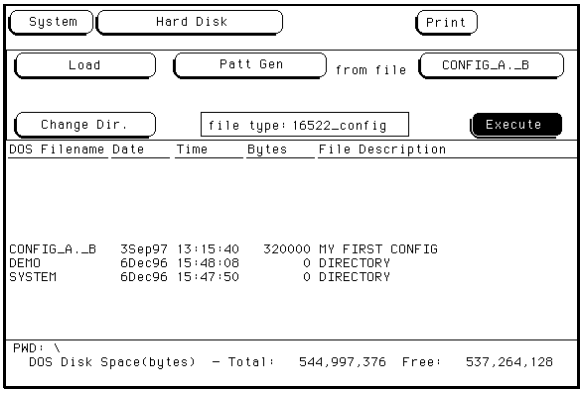
Once you have completed configuring the pattern generator, you can save that configuration to hard disk for future uses.

1. From the System menu, select Configuration.
2. Select Hard Disk.
3. Select the Store operation, then Patt Gen.
4. Select the **to file** field and type a name for the file.
5. Select the **file description** field and type in a description if desired.
6. Select Execute.



To load a configuration

1. From the System menu, select Configuration.
2. Select Hard Disk.
3. Select the Load operation, then Patt Gen.
4. Highlight the file to be loaded by rotating the knob.
5. Select Execute.

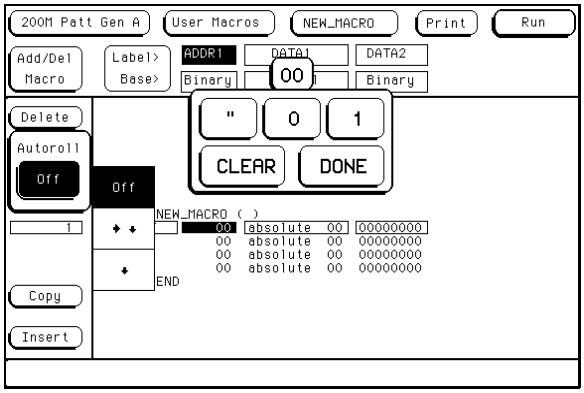


To use Autoroll

When Autoroll is used, each time you complete the process of adding data to a data field, the data entry focus changes to the next specified data field. The data entry keypad remains active, ready to define the next data field.

The following procedure shows you how to use Autoroll:

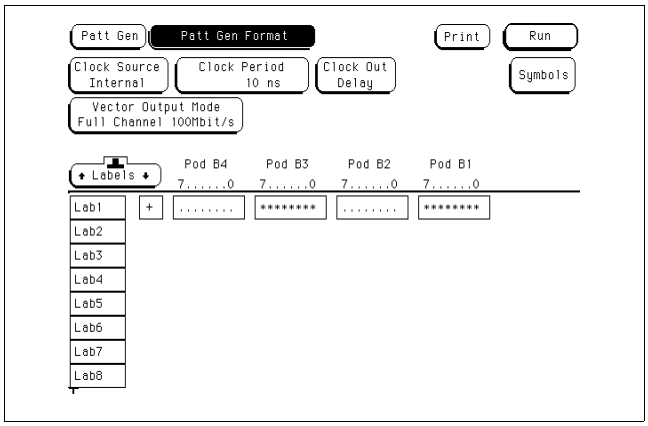
1. Select the first data field to define.
2. Enter the desired data using the pop-up keypad.
3. Select the Autoroll Off field, then select the desired roll direction.



4. As you continue to enter data and select Done, the data field focus rolls to the next data field automatically.

The Format Menu

The Format menu lets you configure the pattern generator with a clock source and parameters, generate a symbol table, select its output mode, assign which vector output channels are used, and then group and label the vector output channels.



Format Menu

Clock Source

The Clock Source field toggles between internal and external. The internal clock source is supplied by the pattern generator and controls the frequency the vectors are output to the system under test.

The external clock is provided by you, or the system under test, and is input to the pattern generator through the CLK IN probe of a clock pod. By using

an external clock, you synchronize the vector output of the pattern generator to the system under test.

Regardless of which clock is selected, vectors are output on the rising edge of the clock.

Clock Period (internal clock source)

This field toggles from Clock Period, when an internal clock source is selected, to Clock Frequency, when an external clock source is selected.

You select clock periods in steps of 1, 2, 2.5, 4, 5, 8, and 10. If the keypad is used to select a value between the step intervals, the value is rounded to the nearest interval.

The minimum clock period available with Vector Output Mode at Full Channel 100 Mbit/s is 10 ns. The minimum clock period available with Vector Output Mode at Half Channel 200 Mbit/s is 5 ns. Maximum clock period for either mode is 250 μs.

Clock Frequency (external clock source)

This field toggles from Clock Frequency, when an external clock source is selected, to Clock Period, when an internal clock source is selected. Set the clock frequency range to match the frequency of the external clock source.

If the Vector Output Mode is Full Channel 100 Mbit/s, you are offered two clock frequency ranges:

- Less than 50 MHz
- Between 50 MHz and 100 MHz

If the Vector Output Mode is Half Channel 200 Mbit/s, you are offered three clock frequency ranges:

- Less than 50 MHz
- Between 50 MHz and 100 MHz
- Greater than 100 MHz

If the external clock is faster than the frequency range selected, the HP 1660CP will produce erroneous output vectors.

Clock Out Delay

The Clock Out Delay setting allows you to position the output clock with respect to data. The zero setting is uncalibrated and should be measured to determine the initial position with respect to the data. Each numerical change of one on the counter results in an approximate change of 1.3 ns.

Symbols

Touching the Symbols field brings up a pop-up menu that lets you build a symbol table to use when putting data into the Sequence and User Macros menus. Providing symbol names to frequently used values lets you enter the values more easily and recognize these values by their symbol name rather than having to remember data values.

Vector Output Mode

The Vector Output Mode determines the channel width, available pods, and the frequency range for both the internal and external clock. The following table shows the difference between the Full Channel 100 MBits/s mode and the Half Channel 200 MBits/s mode.

	Full Channel 100 MBits/s	**Half Channel 200 MBits/s**
Pods Available	Pods 1, 2, 3, 4	Pods 1, 3
Maximum Channels	32; eight per pod	16; eight on pods 1, 3
Maximum External Clock Frequency	100 MHz	200 MHz
Maximum Internal Clock Frequency	100 MHz	200 MHz
Minimum External Clock Frequency	DC	DC
Minimum Internal Clock Frequency	4 kHz	4 kHz

Labels

Labels let the user group output channels from the data pods into a more logical configuration for creating vector data. The pattern generator labels work in the same fashion as the labels for the logic analyzer products, with the exception that an output channel cannot be assigned to more than one label.

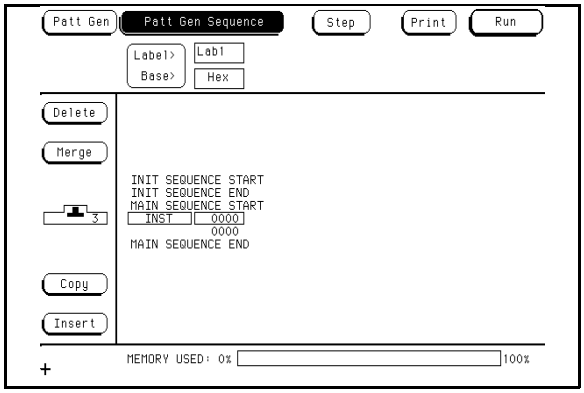
The Sequence Menu

Use the Sequence menu to build your test vector files. There are two sequences, an initialization sequence and a main sequence.

In single run mode, the vectors are output from the first vector in the initialization sequence to the last vector of the main sequence. The last vector of the main sequence will be held at the outputs until run is executed again.

In repetitive run mode, the vectors in the initialization sequence will be output from first to last one time, then the main sequence will repetitively output the vectors in the sequence until the stop field is pressed. The vector being output when stop is acknowledged by the module will be held at the outputs until run is executed again.

The initialization sequence can be empty in which case it will be ignored. The main sequence must contain at least two vectors to output.



Sequence Menu

INIT and MAIN Sequences

Use the knob to highlight individual lines in either vector sequences. When a line is highlighted, you can add data lines below it by selecting the Insert field. Selecting the INST field brings up a dialog box that lets you insert one of the instructions or user macros into the vector sequence.

An instruction is not allowed on the following vector lines of the sequence:

- The first vector of the INIT sequence.
- The first vector of the MAIN sequence.
- The last vector of the MAIN sequence.
- The vector prior to the IF block.
- The first vector of the IF block.
- The last vector of the IF block.
- The vector following the IF block.

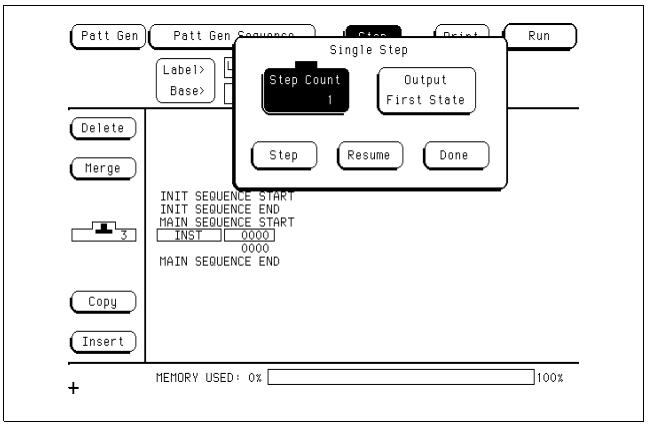
It should be noted that with the Vector Output Mode of Half Channel 200 Mbit/s, the INIT sequence must contain a number of vectors that is divisible by four. If this is not the case, the first vector of the INIT sequence is duplicated to create the correct number of vectors.

With the Vector Output Mode of Full Channel 100 Mbit/s and vector frequencies greater than 50 MHz, the INIT sequence must contain an even number of vectors. Again, if this is not the case, the first vector of the INIT sequence is duplicated to create the correct number of vectors.

Step

Use the Step field to step through your vector sequence to debug a critical set of vectors following a break instruction in the program sequence. Stepping will begin at the vector following the break instruction, or the Output First State item can be pressed which will place the first vector of the sequence on the outputs. Stepping will then begin on the second vector of the sequence. When the last vector of the main sequence is encountered while stepping, the next step command places the first vector of the main sequence on the outputs.

When stepping through a sequence, breaks are ignored while valid branch and wait conditions are executed.



The Step Count Field

The Step Count field lets you set the number of steps to be executed, to a maximum of 100,000. The Output First State field reloads the hardware if necessary and places the first vector of the sequence on the outputs. The Resume field closes the Step pop-up menu and restarts the hardware without changing the previous run mode. Execution resumes from the point at which the sequence was stopped.

Delete

The Delete field lets you delete sequence lines. The From and To fields in the Delete pop-up menu lets you select line numbers with either the knob or another pop-up menu that appears when the From and To fields are selected twice.

When deleting vector rows, the INIT START, INIT END, MAIN START, and MAIN END cannot be deleted. Deleting all the vector rows from INIT START to MAIN END will reset the sequence to the powerup state. The deletion will not be performed if the results of the delete operation will place fewer than two vectors in the main sequence, or, if the delete operation will place an instruction on any of the following vectors:

- The first vector of the INIT sequence.
- The first vector of the MAIN sequence.
- The last vector of the MAIN sequence.
- The vector prior to the IF block.
- The first vector of the IF block.
- The last vector of the IF block.
- The vector following the IF block.

Merge

Selecting the Merge field brings up a pop-up menu that lets you select sections of a previously created configuration file to merge after the current line in the sequence. The Input Drive field selects between the hard disk or the front floppy disk (if present). The Filename field displays a file browser pop-up menu that allows searching for the file to be used in the merge. The Merge Section field lets you select the section of the configuration to be merged. Configuration sections consist of the main sequence and any macros that were created. The merge will not be performed in the following cases:

- Merge data exceeds the maximum number of sequence lines.
- Merge data requires more repeats than are available.
- Merge data requires more macro calls than are available.

Merge is not allowed in the following cases:

- Within a repeat loop.
- Within an IF block (starting with the vector prior to the if, and ending with the vector following the IF).
- Between the start and first vector of the main sequence.
- After the last vector of the main sequence.
- Between the init and main sequence.
- Between the start and first vector of the init sequence.
- Within an empty init sequence (insert one vector in the init and merge after that vector).

Copy

Selecting the Copy field brings up a pop-up menu that lets you select vector sequence lines to be copied and a location to insert them. The values in the Start, End, and Copy After fields can be selected with the knob or with the pop-up keypad that appears when the appropriate field is selected twice.

Copy will not be performed if you run out of macro calls (1000) or repeats (1000). Copy will not be allowed if the result of the copy places an instruction on one of the following vectors:

- The first vector of the INIT sequence.
- The first vector of the MAIN sequence.
- The last vector of the MAIN sequence.
- The vector prior to the IF block.
- The first vector of the IF block.
- The last vector of the IF block.
- The vector following the IF block.

Insert

Selecting the Insert field adds another instruction line immediately below the line that is currently highlighted.

Instructions

User Macro The User Macro instruction brings up a list of current user macros you can insert. Macros are inserted at the current line and expanded at run time.

If the macro selected has parameters, a second pop-up menu will be displayed to allow setting of the passed parameter values. Parameters are passed as 32 bit values and the most significant bits are truncated when the data is applied to labels with less than 32 bits.

Once inserted, the passed parameters of a macro may be altered by selecting that macro again and changing the data. A macro can only be removed from the sequence by using the delete field.

Repeat Loop The Repeat Loop instruction inserts the start and end of a repeat loop using the current vector row as the data. Once the loop has been created, vectors can be inserted or copied into the loop to change the size. A repeat loop will be expanded at run time into individual vectors. The number of repetitions of the loop (maximum 20000) is set when the repeat is first inserted into the sequence and can be altered by selecting the start of the repeat to get the Repeat Count pop-up menu. Both the start and end of a repeat loop will be removed from the sequence if either is included in the delete block.

Break The Break instruction causes a break at the current vector. In single run mode, this instruction halts the sequence and holds the outputs at the break vector's value. In repetitive run mode, this instruction pauses the sequence at the current vector momentarily, then continues.

> When operating at 200 MHz you can not have 2 Break events in succession. This also includes the Wait event.

Signal IMB The Signal IMB instruction creates a signal for the IMB bus of the HP 1660CP at the current vector, allowing the pattern generator to trigger the state or timing analyzers. Multiple signal IMB instructions may be placed in the sequence, but only the first signal IMB will be executed.

Wait Event The Wait Event instruction halts the execution of the program sequence until the event is received by the hardware. Selecting this instruction brings up a pop-up menu that lets you set four data patterns and select one of them or an IMB signal as the event the pattern generator is waiting for.

An external wait event is the ORing of the three input lines on the clock pod. The first wait IMB is the only one recognized because IMB does not allow pulsing.

When operating at 200 MHz you can not have 2 Wait events in succession. This also includes the Break event.

If Event The If Event instruction is only available in Full Channel 100 Mbit/s mode with clock frequencies of 50 MHz and lower. Only one If Event is allowed in a sequence program. If a new if instruction is placed in a program sequence, a message will appear stating that only one if instruction is allowed. To add a new if instruction, the old one must be deleted.

The If event uses either the IMB or the same external clock pod input lines as the Wait event. If the condition is true at the If event, then the data in the If block is output, otherwise it is skipped.

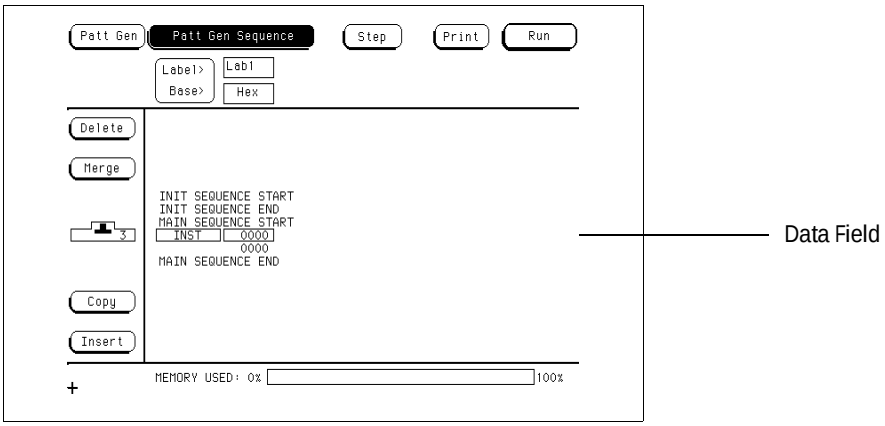
The If event takes the current data line and duplicates as in the following example:

```
current data
        IF
          current data
          current data
        END IF
current data
```

These vectors are now restricted. They cannot have instructions. Delete and Copy operations that result in instructions being placed on these vectors will not be allowed. The If can be removed by deleting either the start or end of the If block.

Data Field

Selecting the data field to the right of the instruction field lets you insert vector data. ASCII-based data cannot be edited, and ASCII- and Symbols-based data cannot be autorolled.



The Sequence Menu with the Data Field Called Out

Autoroll

The Autoroll field is provided to reduce the number of keystrokes required to enter data into the sequence or a macro. When a data field is edited (except in the last vector row), the Autoroll field appears to the left of the data entry pop-up menu. Autoroll can move from left to right across the labels on the display with an automatic line feed, or it can move down a label from vector row to row. When the last vector row of the sequence is encountered, Autoroll will stop the editing process, or the Autoroll can be halted at any point in the editing process by turning the autoroll function off.

Memory Used

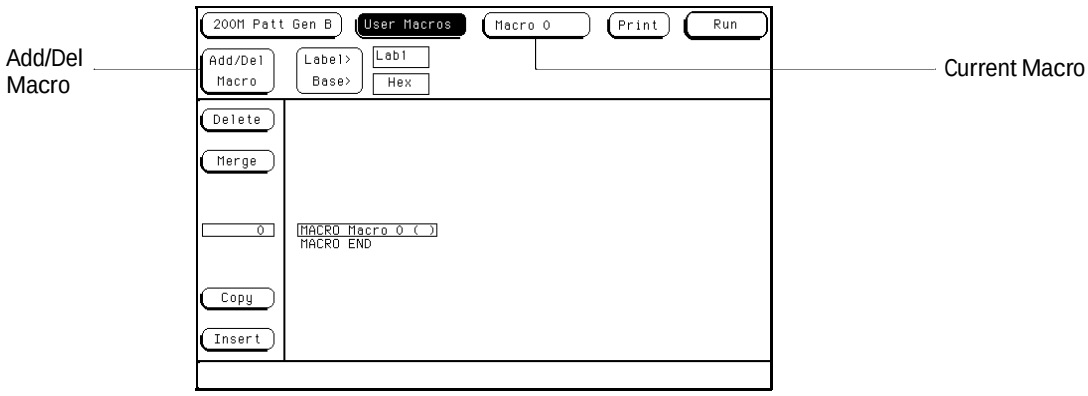
The MEMORY USED bar shows in percent how much memory is being used by the vector sequence entered. It should be noted that Repeat Loops and User Macros may suddenly increase the amount of memory used because they are expanded at run time. It is critical to use the MEMORY USED ‘bar to obtain an idea of how much memory will be needed at run time.

The User Macros Menu

The User Macros menu is used to create new macros and edit existing macros. Macro 0 is the default macro and always exists. Macros let you define a pattern sequence once, then insert the macro by name wherever it is needed.

Macros can also have parameters passed to them. Parameters let you create a generic macro. For each instance of a macro, you specify unique values for the parameterized variable. Each macro can have a maximum of 10 parameters. A maximum of 100 different macros can be defined for use in a single stimulus program.

Differences between User Macros and the INIT and MAIN sequences are that macros cannot use the If instruction, and a macro cannot call another macro.



The User Macor Menu

This section only covers the two unique fields in the User Macros menu and using parameters. For information about other fields in this menu, refer to the discussion of these fields in the previous section on the Sequence Menu.

Macro 0 (current macro field)

Touching this field brings up a list of macros that have been created and are available to insert into the Sequence menu. If you want to edit or view a previously built macro, select that macro from the list and it will appear in the main part of the display.

Add/Delete Macro

Selecting this field brings up a pop-up menu that lets you choose between adding a new macro or deleting one. If you select Add Macro, a new blank macro appears in the display with a new Macro "n" name.

To rename the new macro, select the macro name field, and in the pop-up menu that appears, type in a new name. You can also add parameters to the new macro in the same pop-up menu. For more information on parameters, refer to "Using Parameters" below.

If you select Delete Macro, you will be presented with a list of current macros. Select the macro you want to delete from the list. If the macro you delete is being used in the MAIN sequence, it will be removed from the sequence. If you try to delete the first macro, it will be removed from the MAIN sequence but not from the macro list.

Using Parameters

Parameters are used to pass values into macros. A major benefit in passing parameters is that you keep a macro's functionality generic and still direct specific action identified by parameters. Think of parameters as the only part of a macro that changes as the macro is reused.

You create the macro and add parameters to the macro in the User Macro menu. You then insert the macro and assign parameter values in the Sequence menu. As you reuse the macro in other places in the sequence, simply change parameter values to the new specific values.

Macro parameters are passed as 32-bit values. If fewer than 32 bits are assigned to a label in the Format menu, the most significant bits of the parameter value are truncated when the parameter is used as data for the given label.

Loading ASCII Files

You can create pattern generator files and load them as ASCII files using one of the remote communication interfaces or by loading an ASCII disk file.

Regardless of the load method selected, the general format of the file must conform to certain guidelines. In general, an ASCII file consists of a block of setup information (clock specs, labels, etc.) followed by a block of pattern generator data.

There are a few minor differences between the format required for a communication download and that of a disk file load.

Disk files are loaded into the pattern generator using the LOAD command on the disk menu.

Some general restrictions are:

- Data is assumed to be entirely hexadecimal base.
- No instructions are allowed in the data.
- No macros are defined or invoked in the data.
- All labels consist of adjacent bits.

A special "`ASCII  000000`" string is required to uniquely identify an ASCII disk file. This string cannot be used when loading ASCII files using one of the remote communication interfaces. This line must be the first line of the disk file. It consists of 5 blanks and 6 zeros.

ASCII File Commands

In addition to the unique ASCII file commands described here, you may want to include some standard FORMat commands in the ASCII file, such as those that are used to specify the clock or output mode.

The only FORMat commands that are permitted are FORMat: MODe, CLOCk, and DELay. Refer to the command descriptions in this chapter for the syntax of these commands.

Note that there is no section header prefix for these ASCII file command strings.

Refer to the example programs at the end of this chapter for usage examples of the various commands described in this chapter.

ASCDown Command

Command

ASCDown

The ASCDown command is used to signal the start of an ASCII file load. It causes the current pattern generator label and sequence structures to be cleared and reset to a default state.

The ASCDown command must precede any label definitions and the data portion of an ASCII file load.

Example

```
ASCDown
```

LABel

Command `LABel <name_str>,<width>`

`<name_str>` label string, six characters maximum in length.

`<width>` integer number of bits in the label (1 through 32).

The LABel command is a special means of specifying labels for use by an ASCII file. The label bits are assigned from most to least significant bits across the output pods. Labels may only contain adjacent bits. The user must specify the label string and the width of the field. The label base is hexadecimal.

There is a maximum of 126 labels. No label may be more than 32 bits wide. If a label is too wide (too many bits) for the remaining unused pattern generator bits, it will be discarded. Use of the FORMat:LABel command after the ASCDown command will generate an error.

Example

```
LABel 'TEST1',7

LABel 'ADDR',13
```

VECTor

Command `VECTor <char_count>`

`<char_count>` a ten character string starting with a '#8' and including the total file size count.

The VECTor command is used after the end of the header/setup commands to signal the start of the actual pattern generator data in an ASCII file.

The VECTor command is used with a parameter that specifies the exact byte count of the data block. This count must include all data characters, all blank characters, and all line termination (DOS `cr/lf` or UNIX `cr`) characters. The file character count is the sole criteria used to determine when the bus file transfer is complete. If a disk file is used, the character count has no meaning and can be any value or deleted from the command string.

If the file character count does not match the actual data byte count of the file, an error condition will occur. If the actual data count exceeds the byte count passed in with the VECTor command, excess data will be lost (and treated as remote control bus command(s)). If the actual data count is less than the data count passed in with the VECTor command, the bus transfer will appear to hang while the HP 1660CP system waits for the 'remaining' data. The controller sending the file may, or may not, time-out and terminate the bus transfer. Generally, recovery from this condition involves sending more data until the data byte count is satisfied.

The file character count is contained in a string with a specific format. The actual count is right justified in a ten-character string that starts with a '#8' followed by eight digits. These ten characters are NOT part of the file character count.

The following page shows an example of this.

No data is allowed in the same line as the VECTor command. The line termination in the VECTor command line is included in the character count for the file.

The <char_count> field is not required as part of the VECTor command when creating a disk file, and will be ignored if included.

Example

```
VECTor #800010457
```

Vector Data

The data portion of the ASCII file is basically an array of hexadecimal data fields. Each row of the array corresponds to a single line of the main program. Each column of the array corresponds to a single label as defined on the format menu.

Data fields are separated by one or more blank characters. A line termination (carriage return or carriage return + line feed) signals the end of a line and the start of a new line. If a data field has more data than the label width would indicate, only the least significant bits of the data field are used. If there are more data fields in a row than there are labels, the extra data fields (last data fields in the row) are ignored. If there are fewer data fields in a row than there are labels, the data for the extra (right-most) labels will be zero.

Data lines consisting of only line termination characters are ignored.

The MAIN SEQUENCE must have at least two data lines. In the ASCII data file, a row consisting of only '*M' is used to signal the start of the main sequence. If there is to be no data in the init sequence, the first row of the file after the VECTor command must be '*M'. Note that the quotes in '*M' are not really in the file. The line termination after the '*M' (as well as the '*M') must be included in the character count for a file loaded using a remote bus.

Any characters that are not valid hexadecimal digits (0 through 9, or upper/lower case a through f) are ignored and treated as field separators. This could cause problems if a typo appears in the middle of a data value (for example, '12R4' will be assigned to two labels as '12' and '4').

The last data row of the file must end with a line termination as this is the flag to load the data row into the data structure. Failure to do this will result in a short main program.

When counting file characters be aware of how a particular file generator (editor) terminates a line. DOS-based systems use two characters. Be sure to account for line termination character(s) in the overall file character count.

The ASCII file load mechanism assumes correctness in the data file and any header commands. Error handling is rather basic, and treating unexpected characters as field separators could create bizarre results when parsing the file. Error messages point to the line number where the parser thinks the error occurred, but the line count may not be exact because of parsing problems with the data.

When using a LAN interface to send ASCII data, an extra line feed <lf> is required at the end of the file. This <lf> is NOT included in the <char_count> value. It is required to ensure the data buffer is flushed.

Serious problems will cause the default main program to be loaded in an effort to avoid locking up the HP 1660CP system.

FORMat:xxx

Command

```
FORMat:MODE
FORMat:CLOCk
FORMat:DELay
```

These commands transfer set fields from the Format menu. The existing clock scheme is used if nothing is specified here. Command syntax is same as normal bus commands.

Examples

```
FORMat:MODE FULL
FORMat:CLOCk INT,5E-9
FORMat:DELay 1E-9
```

Loading an ASCII file over a bus (example)

To load an ASCII file over the bus use the following example. A few items to be noted:

- Line numbers are added for documentation only and are NOT part of the actual remote bus commands.
- In this example, the string `'<lf>'` is a generic line feed sequence and counts as a single character.

```
010  SELect <slot><lf>

020  ASCDOWN<lf>

030  FORM:MODE FULL<lf>

040  LABEL 'LAB1',8<lf>
041  LABEL 'DATA',8<lf>
042  LABEL 'TEST',9<lf>
043  LABEL 'CLK',3<lf>
044  LABEL 'BIG',12<lf>

050  VECT #800000092<lf>
060  12 34 56 7 89A<lf>
070  0 22 7 0 FFF<lf>
080  A0 33 00 1 111<lf>
090  *M<lf>
100  92 6F 00 1 FF0<lf>
110  CA CA 00 1 00F<lf>
120  00 10 11 0 ABC<lf>
```

Notes

- Lines 010 through 044 can be sent as discrete remote control commands or included in a single file (with the data) and loaded using the bus.
- Other format commands could be used in place of or in addition to line 030.
- The label sequence seen in lines 040 through 044 will result in a specific bit assignment. A different ordering of the LABel commands would give a different ordering to the bits.

- There is a space before the '#8' in line 050.
- The character count in line 050 is based on:
  - 15 characters (10 digits, 4 blanks, 1 <lf>) each in lines 060, 080, 100, 110, and 120
  - 3 characters in line 090
  - 13 characters in line 070
  - 1 character (the <lf>) in line 050

Format Specification

Clock Source: Internal

Vector Output Mode: Full Channel 100 Mbit/s

Clock Period: 10 ns

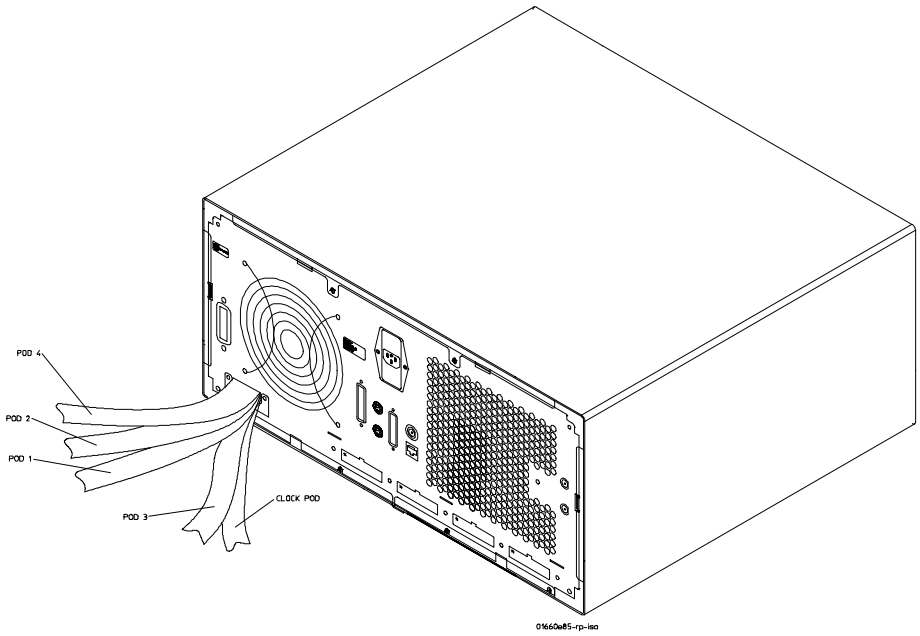
Clock Out Delay Setting: 0

Pattern Generator Probing System

This section discusses the probing system for the Pattern Generator.

Pod Numbering

The HP 1660CP pods are numbered as shown in the figure below.



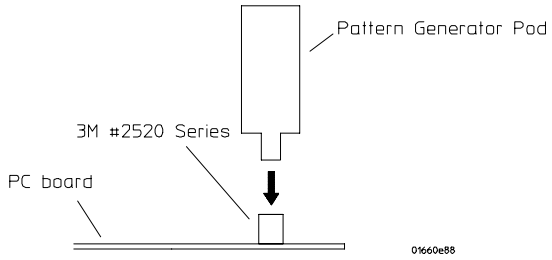
HP 1660CP Pattern Generator Pods

Connecting Pods Directly to a PC Board

To connect the pattern generator pods directly to the PC board, use one of the following two methods. Both methods require that a 3M 2520-series, or similar alternative connector be installed on the PC board.

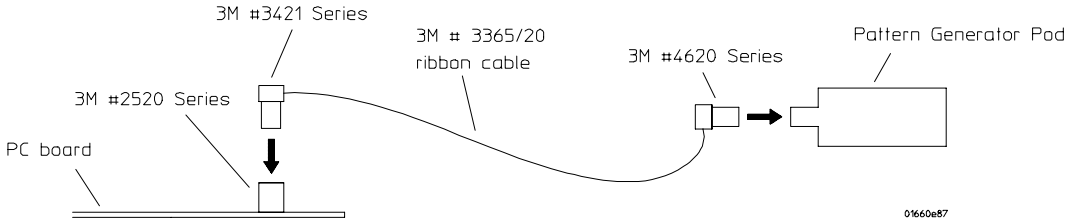
Direct pod to board connection

Simply plug the pod directly into the 3M 2520-series, or similar alternative connector on the PC board.



Jumper cable to pod connection

Use this method when you have clearance problems on the PC board. Construct a flat ribbon cable and connect as shown below.



Equivalent connectors can be obtained from sources other than 3M.

Output Pod Characteristics

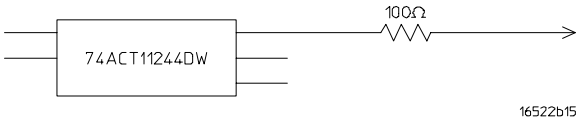
The following equivalent circuit information is provided to help you select the appropriate clock and data pods for your application.

HP 10461A TTL Data Pod

Output type	10H125 with 100 ohm in series
Maximum clock	200 MHz
Skew	Typical <2 ns; worst case 4 ns (see note 1)
Recommended lead set	HP 10474A

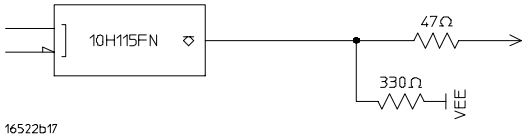
HP 10462A 3-State TTL/CMOS Data Pod

Output type	74ACT11244 with 100 ohm in series 10H125 on non 3-state channel 7 (see note 2),
3-state enable	negative true, 100K ohm to GND, enabled on no connect
Maximum clock	100 MHz
Skew	Typical <4 ns; worst case 12 ns (see note 1)
Recommended lead set	HP 10474A



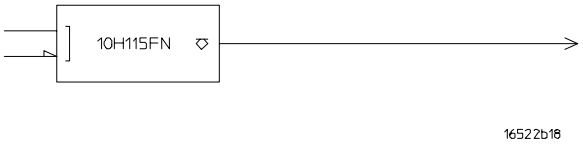
HP 10464A ECL Data Pod (terminated)

Output type	10H115 with 330 ohm pulldown, 47 ohm in series
Maximum clock	200 MHz
Skew	Typical <1 ns; worst case 2 ns (see note 1)
Recommended lead set	HP 10474A



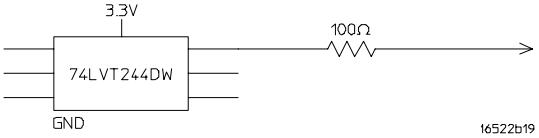
HP 10465A ECL Data Pod (unterminated)

Output type	10H115 (no termination)
Maximum clock	200 MHz
Skew	Typical <1 ns; worst case 2 ns (see note 1)
Recommended lead set	HP 10347A



HP 10466A 3-State TTL/3.3 Volt Data Pod

Output type	74LVT244 with 100 ohm in series 10H125 on non 3-state channel 7 (see note 2)
3-state enable	negative true, 100K ohm to GND, enabled on no connect
Maximum clock	200 MHz
Skew	Typical <3 ns; worst case 7 ns (see note 1)
Recommended lead set	HP 10474A

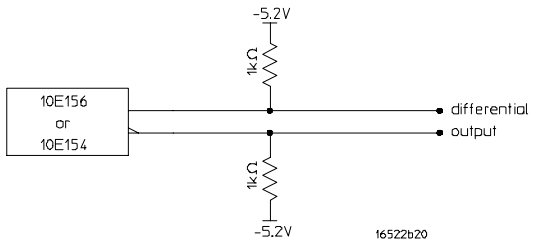


Note 1 Typical skew measurements made at pod connector with approximately 10 pF/50K ohm load to GND; worst case skew numbers are a calculation of worst case conditions through circuits.

Note 2 Channel 7 on the 3-state pods has been brought out in parallel as a non 3-state signal. By looping this output back into the 3-state enable line, the channel can be used as a 3-state enable.

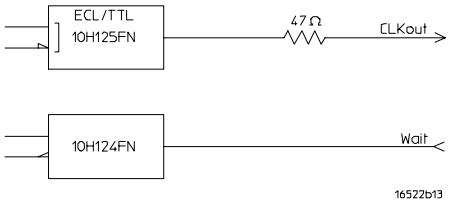
Data Cable Characteristics Without a Data Pod

The HP 1660CP data cables without a data pod provide an ECL-terminated (1 KΩ to -5.2 V) differential signal. These are usable when received by a differential receiver, preferably with a 100-ohm termination across the lines. These signals should not be used single ended due to the slow fall time and shifted voltage threshold (they are not ECL compatible).



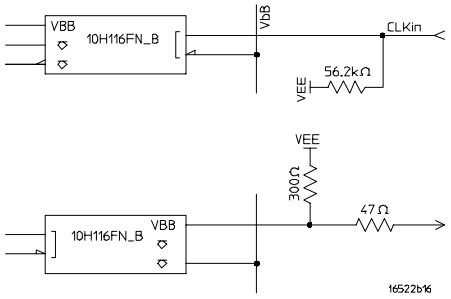
HP 10460A TTL Clock Pod

Clock output type	10H125 with 47 ohm series; true & inverted
Clock output rate	100 MHz maximum
Clock out delay	11 ns maximum in 9 steps
Clock input type	TTL - 10H124
Clock input rate	DC to 100 MHz
Pattern input type	TTL - 10H124 (no connect is logic 1)
Clk-in to clk-out	Approx. 30 ns
Patt-in to recognition	Approx. 15 ns + 1 clk period
Recommended lead set	HP 10474A



HP 10463A ECL Clock Pod

Clock output type	10H116 differential unterminated; and differential with 330 ohm to -5.2v and 47 ohm series
Clock output rate	200 MHz maximum
Clock out delay	11 ns maximum in 9 steps
Clock input type	ECL - 10H116 with 50 KΩ to -5.2 V
Clock input rate	DC to 200 MHz
Pattern input type	ECL - 10H116 with 50 KΩ (no connect is logic 0)
Clk-in to clk-out	Approx. 30 ns
Patt-in to recognition	Approx. 15 ns + 1 clk period
Recommended lead set	HP 10474A



6

Triggering Examples

Triggering Examples

As you begin to understand a problem in your system, you may realize that certain conditions must occur before the problem occurs. You can use sequential triggering to ensure that those conditions have occurred before the analyzer recognizes its trigger and captures information.

If you are not familiar with the trigger menus, read through Chapter 4, "Using the Trigger Menu," and try working through the examples in the Logic Analyzer Training Kit manual.

Single-Machine Trigger Examples

The following examples require only a single analyzer to make measurements. Sequence specifications are given in the form you see within the sequence levels, but the illustrations show the complete, multi-level sequence specification.

Although all the examples are case-specific, terms are named in a way that highlights their role in solving the trigger problem. You can easily apply the examples to your specific instance by changing the specific values assigned to the trigger terms.

To store and time the execution of a subroutine

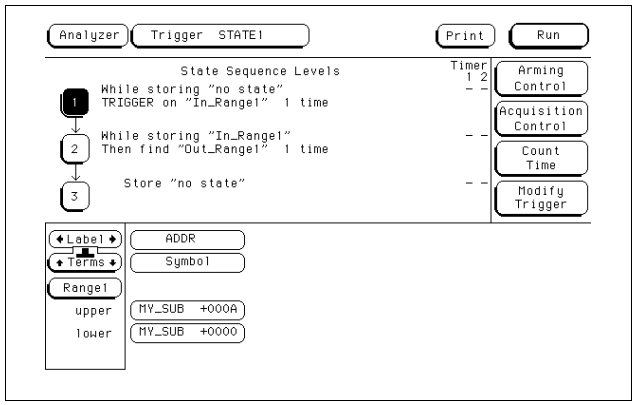
Most system software of any kind is composed of a hierarchy of functions and procedures. During integration, testing, and performance evaluation, you want to look at specific procedures to verify that they are executing correctly and that the implementation is efficient. The analyzer lets you do this by triggering on entry to the address range of the subroutine and counting the elapsed time since the trigger state.

1. Go to the state analyzer's Trigger menu.
2. Set Count to Time.
3. Define a range term, such as Range1, to represent the address range of the particular subroutine.

   You may need to examine the structure of your code to help determine this. If your subroutine calls are really procedure calls, then there is likely to be some code at the beginning of the routine that adjusts the stack for local variable allocation. This will precede the address of the first statement in the procedure. If your subroutine has no local storage and is called by a jump or branch, then the first statement will also be the entry address.
4. Under State Sequence Levels, enter the following sequence specification:
   - While storing "no state" TRIGGER on "In_Range1" Occurs 1 Else on "no state" go to level 1
   - While storing "In_Range1" Then find "Out_Range1" Occurs 1 Else on "no state" go to level 2
   - Store "no state" on "no state" go to level 1

For processors that prefetch instructions or have pipelined architectures, you may want to add part or all of the depth of the pipeline to the start address for In_Range1 to ensure that the analyzer does not trigger on a prefetched but unexecuted state.

The figure below shows what you would see on your analyzer screen after entering the sequence specification given in step 4.



Trigger Setup for Storing and Timing Execution of a Subroutine

Suppose you want to trigger on entry to a routine called MY_SUB. You can create a symbol from the address of MY_SUB in the Format menu, allowing you to reference the symbol name when setting up the trace specification. Assume that MY_SUB extends for 0A hex locations. You can set up the trigger sequencer as shown in the display.

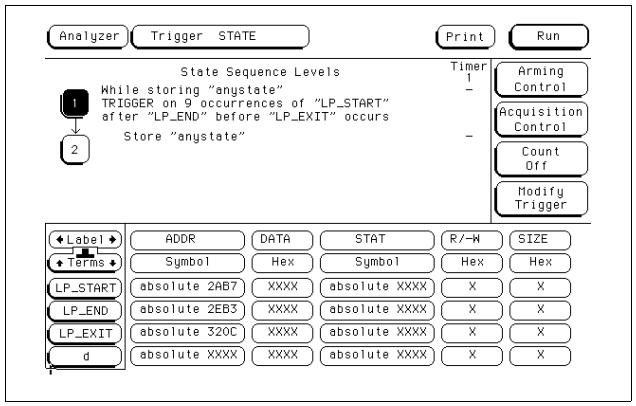
To trigger on the nth iteration of a loop

Traditional debugging requires print statements around the area of interest. This is not possible in most embedded systems designs, but the analyzer lets you view the system's behavior when a particular event occurs. Suppose that your system behaves incorrectly on the last iteration of a loop, which, in this instance, happens to be the 10th iteration. You can use the analyzer's triggering capabilities to capture that iteration and subsequent processor activity.

1. Go to the state analyzer's Trigger menu.
2. Define the terms LP_START and LP_END to represent the start and end addresses of statements in the loop, and LP_EXIT to represent the first statement executed after the loop terminates.
3. Change State Sequence Level 1's macro to "Find event2 n times after event1 before event3 occurs."
4. In the pop-up, enter the following sequence specification:

   - While storing anystate Find "LP_START" "9" times after "LP_END" before "LP_EXIT" occurs.

   You should use your value for n-1 instead of "9" in the sequence specification above.



Trigger Setup for Triggering on the 10th Iteration of a Loop

The specification has some advantages and a potential problem.

- The advantages are that a pipelined processor won't trigger until it has executed the loop 10 times. Requiring LP_END to be seen at least once first ensures that the processor actually entered the loop; then, 9 more iterations of LP_START is really the 10th iteration of the loop. Also, no trigger occurs if the loop executes less than 10 times – the analyzer sees LP_EXIT and restarts the trigger sequence.
- The potential problem is that LP_EXIT may be too near LP_END and thus appear on the bus during a prefetch. The analyzer will constantly restart the sequence and will never trigger. The solution to this problem depends on the structure of your code. You may need to experiment with different trigger sequences to find one that captures only the data you want to view.

To trigger on the nth recursive call of a recursive function

1. Go to the state analyzer's Trigger menu.
2. Define the terms CALL_ADD, F_START, and F_END to represent the called address of the recursive function, and the start and end addresses of the function. Define F_EXIT to represent the address of the first program statement executed after the original recursive call has terminated.

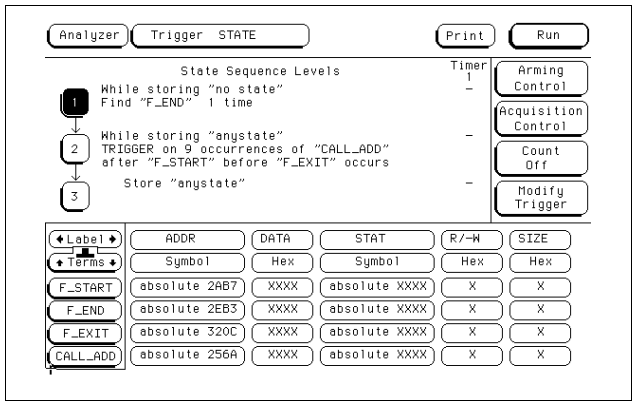
   Typically, CALL_ADD is the address of the code that sets up the activation record on the stack, F_START is the address of the first statement in the function, and F_END is the address of the last instruction of the function, which does not necessarily correspond to the address of the last statement. If the start of the function and the address called by recursive calls are the same, or you are not interested in the function initialization code, you can use F_START for both CALL_ADD and F_START.
3. Change State Sequence Level 1's macro to "Find event2 n times after event1 before event3 occurs."
4. In the pop-up, enter the following sequence specification:

   - While storing anystate Find "CALL_ADD" "9" times after "F_START" before "F_EXIT" occurs.

   You should use your value for n-1 instead of "9" in the specification.
5. Insert another sequence level before the current one. Select the User Level macro and enter the following specification:

   - While storing "no state" Find "F_END" occurs "1" Else on "no state" go to level 1.

   As with the trigger specification for "To trigger on the nth iteration of a loop," this specification helps avoid potential problems on pipelined processors by requiring that the processor already be in the first recursive call before advancing the sequencer. Depending on the exact code used for the calls, you may need to experiment with different trigger sequences to find one that captures only the data you want to view.



Triggering on the 10th Call of a Recursive Function

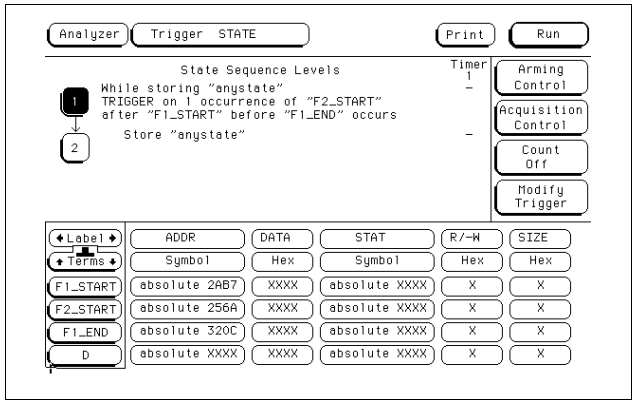
To trigger on entry to a function

This sequence triggers on entry to a function only when it is called by one particular function.

1. Go to the state analyzer's Trigger menu.
2. Define the terms F1_START and F1_END to represent the start and end addresses of the calling function. Define F2_START to represent the start address of the called function.
3. Change State Sequence Level 1's macro to "Find event2 n times after event1 before event3 occurs."
4. In the pop-up menu, enter the following sequence specification:
   - While storing anystate Find "F2_START" "1" times after "F1_START" before "F1_END" occurs.

   This sequence specification assumes there is some conditional logic in function F1 that chooses whether or not to call function F2. Thus, if F1 ends without the analyzer having seen F2, the sequence restarts.

   The specification also stores all execution inside function F1, whether or not F2 was called. If you are interested only in the execution of F1, without the code that led to its invocation, you can change the storage specification from "anystate" to "nostate" for the second sequence term.

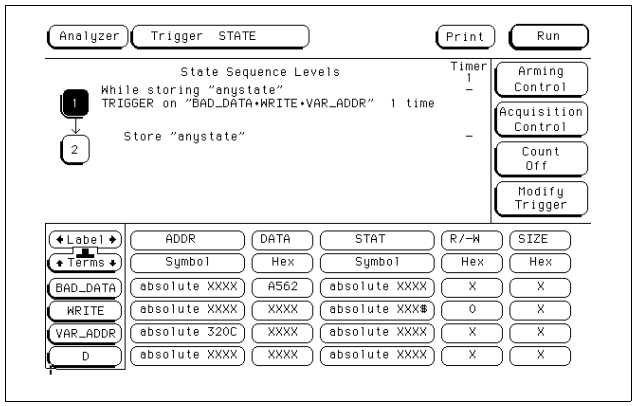


Triggering on Entry to a Function

To capture a write of known bad data to a particular variable

The trigger specification ANDs the bad data on the data bus, the write transaction on the status bus, and the address of the variable on the address bus.

1. Go to the state analyzer's Trigger menu.
2. Define the terms BAD_DATA, WRITE, and VAR_ADDR to represent the bad data value, write status, and the address of the variable.
3. Under State Sequence Level 1, enter the following sequence specification (use the Combination trigger term):
   - While storing "anystate" TRIGGER on "BAD_DATA • WRITE • VAR_ADDR" Occurs "1" Else on "no state" go to level "1"



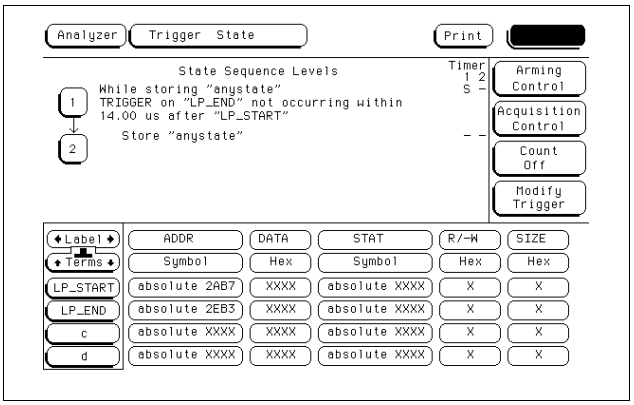
Capturing a Bad Write to a Variable

To trigger on a loop that occasionally runs too long

This example assumes the loop normally executes in 14 µs.

1. Go to the state analyzer's Trigger menu.
2. Define terms LP_START and LP_END to represent the start and end addresses of the loop, and set Timer1 to the normal duration of the loop.
3. Change State Sequence Level 1's macro to "Find event2 occurring too late after event1."
4. In the pop-up menu, enter the following sequence specification:
   - While storing anystate Find "LP_END" occurring too late after "LP_START" Use Timer: "Timer1" Time="14 µs"

Of course, you use your normal loop duration in place of "14 µs." The macro will automatically start Timer1 for you.

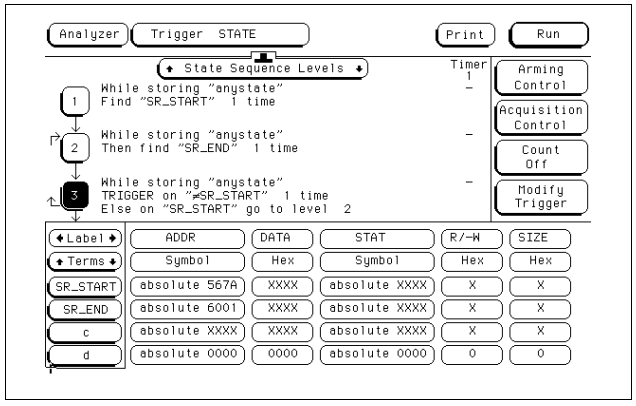


Triggering on a Loop Overrun

To verify correct return from a function call

The exit code for a function will often contain instructions for deallocating stack storage for local variables and restoring registers that were saved during the function call. Some language implementations vary on these points, with the calling function doing some of this work, so you may need to adapt the procedure to suit your system.

1. Go to the state analyzer's Trigger menu.
2. Define terms SR_START and SR_END to represent the start and end addresses of the subroutine.
3. Under State Sequence Levels, insert 2 more sequence levels and enter the following sequence specification:
   - While storing "anystate" Find "SR_START" Occurs "1" Else on "no state" go to level "1"
   - While storing "anystate" Then find "SR_END" Occurs "1" Else on "no state" go to level "2"
   - While storing "anystate" TRIGGER on "≠ SR_START" Occurs "1" Else on "SR_START" go to level "2"

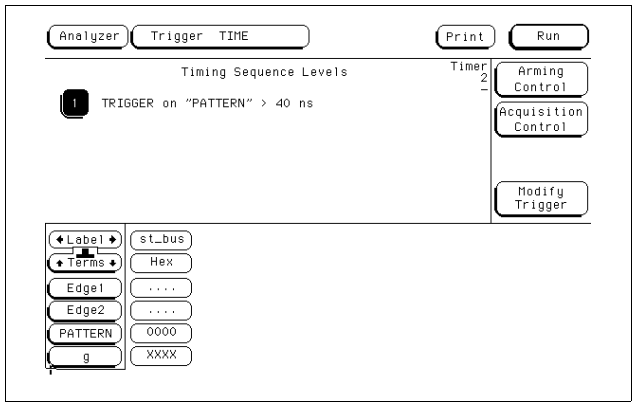


Verifying Correct Return from a Function Call

To trigger after all status bus lines finish transitioning

In some applications, you will want to trigger a measurement when a particular pattern has become stable. For example, you might want to trigger the analyzer when a microprocessor's status bus has become stable during the bus cycle.

1. Go to the timing analyzer's Trigger menu.
2. Define a term called PATTERN to represent the value to be found on the status bus lines.
3. Under Timing Sequence Levels, enter the following sequence specification:
   - TRIGGER on "PATTERN" > 40 ns



Triggering After Lines have Finished Transitioning

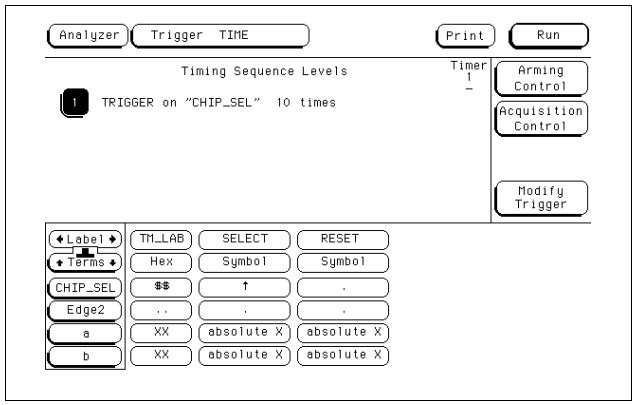
To find the nth assertion of a chip select line

1. Go to the timing analyzer's Trigger menu.
2. Define the Edge1 term to represent the asserting transition on the chip select line.

   You can rename the Edge1 term to make it correspond more closely to the problem domain, for example, to CHIP_SEL.
3. Under Timing Sequence Levels, enter the following sequence specification:

   - TRIGGER on "CHIP_SEL" Occurs "10" Else on "no state" go to level "1"

   You should use your value for "n" in place of "10" in the specification above.

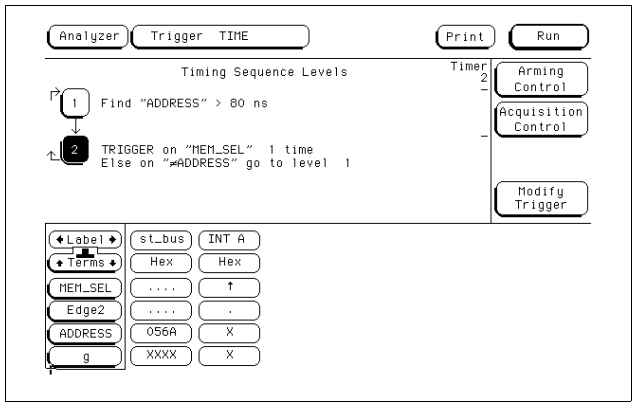


Triggering on the 10th Assertion of a Chip Select Line

To verify that the chip select line is strobed after the address is stable

1. Go to the timing analyzer's Trigger menu.
2. Define a term called ADDRESS to represent the address in question and the Edge1 term to represent the asserting transition on the chip select line.

   You can rename the Edge1 term to suit the problem, for example, to MEM_SEL.
3. Under Timing Sequence Levels, enter the following sequence specification:
   - Find "ADDRESS" > 80 ns
   - TRIGGER on "MEM_SEL" Occurs "1" Else on "≠ ADDRESS" go to level "1"



Verifying SetupTime for Memory Address

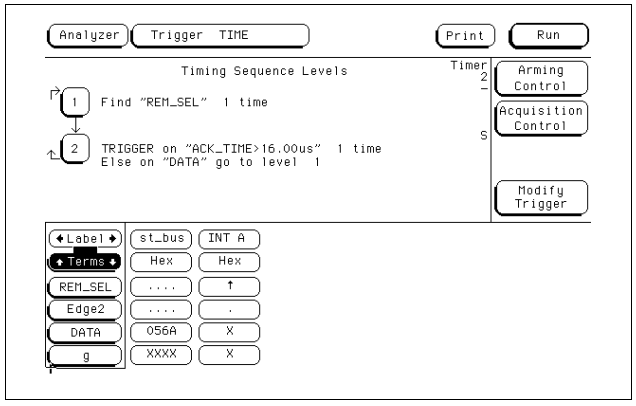
To trigger when expected data does not appear when requested

1. Go to the timing analyzer's Trigger menu.
2. Define a term called DATA to represent the expected data, the Edge1 term to represent the chip select line of the remote device, and the Timer1 term to identify the time limit for receiving expected data.

   You can rename the Edge1 and Timer1 terms to match the problem domain, for example, to REM_SEL and ACK_TIME.
3. Under Timing Sequence Levels, enter the following sequence specification:
   - Find "REM_SEL" Occurs "1" Else on "no state" go to level "1"
   - TRIGGER on "ACK_TIME > 16.00 µs" Occurs "1" Else on "DATA" go to level "1"

   You will need to start ACK_TIME timer (Timer1) upon entering this state. You do this using the Timer Control field in the menu for sequence level 2.

   This sequence specification causes the analyzer to trigger when the data does not occur in 16 µs or less. If it does occur within 16 µs, the sequence restarts. Specifications of this type are useful in finding intermittent problems. You can set up and run the trace, then cycle the system through temperature and voltage variations, using automatic equipment if necessary. The failure will be captured and saved for later review.



Triggering when Data not Returned

To test minimum and maximum pulse limits

1. Go to the timing analyzer's Trigger menu.
2. Define the Edge1 term to represent the positive-going transition, and define the Edge2 term to represent the negative-going transition on the line with the pulse to be tested.

   You can rename these terms to POS_EDGE and NEG_EDGE.
3. Define the Timer1 term to represent the minimum pulse width, and the Timer2 term to represent the maximum pulse width.

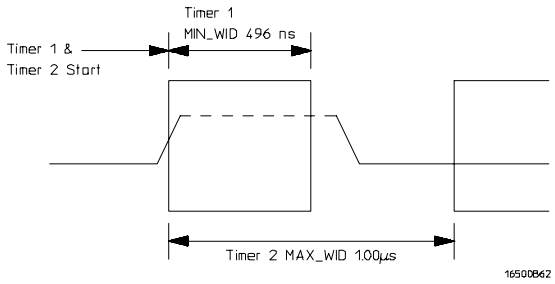
   You can rename these terms to MIN_WID and MAX_WID. In this example, Timer1 was set to 496 ns and Timer2 was set to 1 µs. Both timers start when sequence level 2 is active.
4. Under Timing Sequence Levels, enter the following sequence specification:

   - Find "POS_EDGE" Occurs "1" Else on "no state" go to level "1"
   - Then find "NEG_EDGE" Occurs "1" Else on "no state" go to level "2"

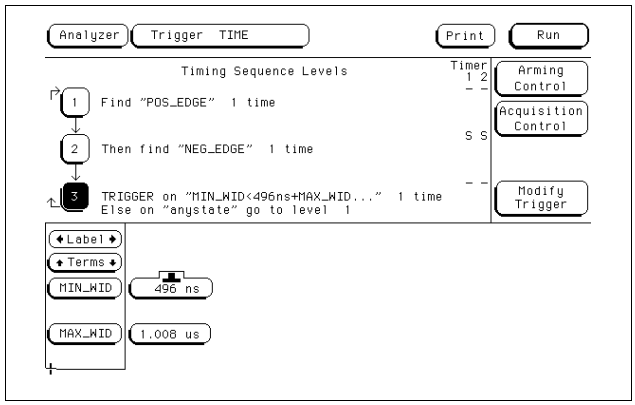
   You will need to start both timers upon entering this second state. You do this using the Timer Control field in the menu for sequence level 2.

   - TRIGGER on "MIN_WID 496 ns + MAX_WID 1.00 µs" Occurs "1" Else on "anystate" go to level "1"

   Because both timers start when entering sequence level 2, they start as soon as the positive edge of the pulse occurs. Once the negative edge occurs, the sequencer transitions to level 3. If at that point, the MIN_WID timer is less than 496 ns or the MAX_WID timer is greater than 1 µs, the pulse width has been violated and the analyzer triggers. Otherwise, the sequence is restarted.



Measurement of Minimum and Maximum Pulse Width Limits

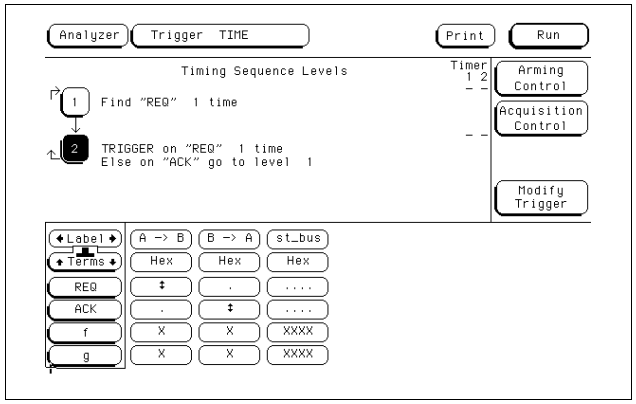


Triggering when a Pulse Exceeds Minimum or Maximum Limits

To detect a handshake violation

1. Go to the timing analyzer's Trigger menu.
2. Define the Edge1 term to represent either transition on the first handshake line, and the Edge2 term to represent either transition on the second handshake line.

   You can rename these terms to match your problem, for example, to REQ and ACK.
3. Under Timing Sequence Levels, enter the following sequence specification:
   - Find "REQ" Occurs "1" Else on "no state" go to level "1"
   - TRIGGER on "REQ" Occurs "1" Else on "ACK" go to level "1"



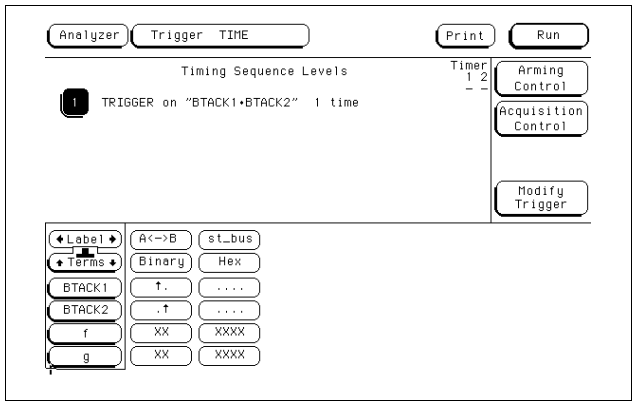
Triggering on a Handshake Violation

To detect bus contention

In this setup, the trigger occurs only if both devices assert their bus transfer acknowledge lines at the same time.

1. Go to the timing analyzer's Trigger menu.
2. Define the Edge1 term to represent assertion of the bus transfer acknowledge line of one device, and Edge2 term to represent assertion of the bus transfer acknowledge line of the other device.

   You can rename these to BTACK1 and BTACK2.
3. Under Timing Sequence Levels, enter the following sequence specification:
   - TRIGGER on "BTACK1 • BTACK2" Occurs "1" Else on "no state" go to level "1"



Triggering onBus Contention

Cross-Arming Trigger Examples

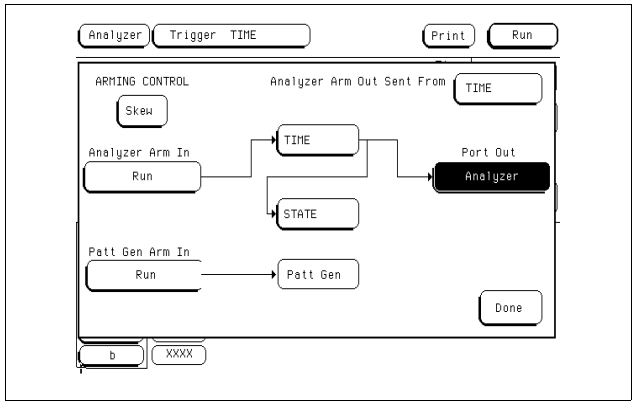
The following examples use cross arming to coordinate measurements between two separate analyzers within the logic analyzer or between analyzers and the pattern generator. The analyzers can be configured as either a state analyzer and timing analyzer, or two state analyzers. It is not possible to set both to timing.

You set up cross arming in the Arming Control menu (obtained by selecting Arming Control in the Trigger menu). When coordinating measurements between two instruments, you need to select Count Time to correlate the measurements.

To examine software execution when a timing violation occurs

The timing analyzer triggers when the timing violation occurs. When it triggers, it also sets its "arm" level to true. When the state analyzer receives the arm signal, it triggers immediately on the present state.

1. Set up one state analyzer and one timing analyzer.
2. Go to the timing analyzer's Trigger menu.
3. Define Edge1 to represent the control line where the timing violation occurs.
4. Under Timing Sequence Levels, enter the following sequence specification:
   - TRIGGER on "Edge1" Occurs "1" Else on "no state" go to level "1"
5. Go to the state analyzer's Trigger menu and check that term "a" is set to "don't care". In the Arming Control menu, set the state analyzer to be run by the timing analyzer.



Arming the State Analyzer from the Timing Analyzer

6. Under State Sequence Levels, enter the following sequence specification:
   - While storing "anystate" TRIGGER on "arm • a" Occurs "1" Else on "no state" go to level "1"

To look at control and status signals during execution of a routine

The state analyzer will trigger on the start of the routine whose control and status signals are to be examined more frequently than once per bus cycle. When the state analyzer triggers, it sends out an arm signal. The timing analyzer triggers when it receives the true arm level and detects the transition represented by Edge1.

1. Set up one state analyzer and one timing analyzer.
2. Go to the state analyzer's Trigger menu and define term R_START to represent the starting address of the routine.
3. Under State Sequence Levels, enter the following sequence specification:
   - While storing "anystate" TRIGGER on "R_START" Occurs "1" Else on "no state" go to level "1"
4. Go to the timing analyzer's Trigger menu.
5. Define the Edge1 term to represent a transition on one of the control signals.
6. Set the timing analyzer to be run by the state analyzer. Under Timing Sequence Levels, enter the following sequence specification:
   - TRIGGER on "arm • Edge1" 1 time

   You do not need to use a combination trigger when one analyzer is armed from the other analyzer – the arm term is ANDed automatically with the term already in use at that level.

To detect a glitch

The following setup uses a state analyzer to capture state flow occurring at the time of the glitch. This can be useful in troubleshooting. For example, you might find that the glitch is ground bounce caused by a number of simultaneous signal transitions.

1. Set up a timing analyzer and a state analyzer.
2. Go to the timing analyzer's Format menu and set the Timing Acquisition Mode to Glitch Half Channel 125 MHz.

   Glitch mode only allows you to use one pod of a pod pair at a time. If the wrong pod is active, toggle by selecting the Pod button.
3. Go to the timing analyzer's Trigger menu.
4. Select an Edge term. Then assign glitch detection "*" to the channels of interest represented by the Edge term.
5. Go to the state analyzer's Trigger menu.
6. Set the analyzer to be armed by the timing analyzer. Leave the trigger set to trigger on any state.

   If you don't see the activity of interest in the state trace, try changing the trigger position using the Acquisition Control field in the Trigger menu of the state analyzer. By changing the Acquisition mode to manual, you can position the trigger at any state relative to analyzer memory.

> The timing analyzer can detect glitch activity on a waveform. A glitch is defined as two or more transitions across the logic threshold between adjacent timing analyzer samples.

To trigger timing analysis of a count-down on a set of data lines

Your target system may include various state machines that are started by system events such as interrupt processing or I/O activity. The state analyzer is ideal for recognizing the system events; the timing analyzer is ideal for examining the step-by-step operation of the state machines.

1. Set up a timing analyzer and a state analyzer.
2. Go to the state analyzer's Trigger menu.
3. Set the timing analyzer to be run from the state analyzer.
4. Set the state analyzer to trigger on the label and term that identify the start of the count-down routine.
5. Go to the timing analyzer's Trigger Menu.
6. Set the timing analyzer to trigger on any state and store any state.

To monitor two coprocessors in a target system

Debugging coprocessor systems can be a complex task. Replicated systems and contention for shared resources increase the potential problems. Using two state analyzers with preprocessors can make it much easier to discover the source of such problems. For example, you may want to set up one analyzer to trigger only when a certain problem occurs, and set up the other analyzer to be armed by the first analyzer so that it takes its trace only when the first analyzer recognizes its trigger. This will let you observe the behavior of both coprocessors during the occurrence of a problem.

1. Set up both analyzers as state analyzers.
2. Go to the first analyzer's Trigger menu.
3. Set the second analyzer to be run from the first analyzer.
4. Turn on "Count Time".
5. Set the first analyzer to trigger on the problem condition.

   Some problems may involve complex sequences of conditions. See earlier examples in this chapter for more information on defining trigger sequences.
6. Go to the Trigger menu of the second analyzer.
7. Check that the second analyzer is triggering on arm and that Count Time is set.

   After the measurement is complete, you can interleave the trace lists of both state analyzers to see the activity executed by both coprocessors during related clock cycles.

   You can use a similar procedure if you have only one processor, but want to monitor its activity with that of other system nodes, such as chip-select lines, I/O activity, or behavior of a watchdog timer. In some instances it may be easier to look at related activity with a timing analyzer.

See Also

"Special Displays" in this chapter.

"To trigger timing analysis of a count-down on a set of data lines" in this chapter.

Interleaved trace lists

Interleaved trace lists allow you to view data captured by two analyzers in a single display. When you interleave the traces, you see each state that was captured by each analyzer. These states are shown on consecutive lines.

You can interleave state listings from state analyzers when two are used together in a run. Interleaved state listings are useful when you are using multiple analyzers to look at interaction between two or more processors. They are also useful when you need more analysis width than is available in one analyzer.

Mixed Display mode

The Mixed Display mode allows you to show state listings and timing waveforms together on screen. State listings are shown at the top of the screen and waveform displays are shown at the bottom. You can interleave state listings from two analyzers at the top of the screen, if desired. You can display waveforms from the timing analyzer at the bottom of the screen.

To interleave trace lists

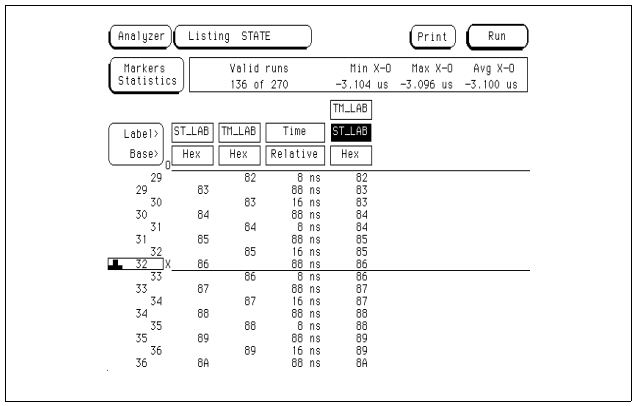
1. Set up both analyzers as state analyzers.
2. Go to the Trigger menu of the first analyzer.
3. Set Count to Time, and set up the trigger.

   The logic analyzer uses the time tags stored with each state to determine the ordering of states shown in an interleaved trace list.
4. Set Count to Time, and set up the trigger on the second analyzer.

   The second analyzer does not need to be run from the first analyzer, but both analyzers must have "Count Time" turned on to correlate the data.
5. Make the measurement run.
6. Go to one of the Listing menus.
7. Select one of the label fields in the trace list display, then select Interleave.
8. Select the name of the other analyzer and the label to interleave.

   Interleaved data is displayed in a light shade. Trace list line numbers of interleaved data are indented. The labels identifying the interleaved data are shown above the labels for the current analyzer, and are displayed in a light shade.

   If you have problems with the procedure, check that each analyzer has an independent clock from the target system.



Interleaved Trace Lists on the HP 1661CP

To view trace lists and waveforms on the same display

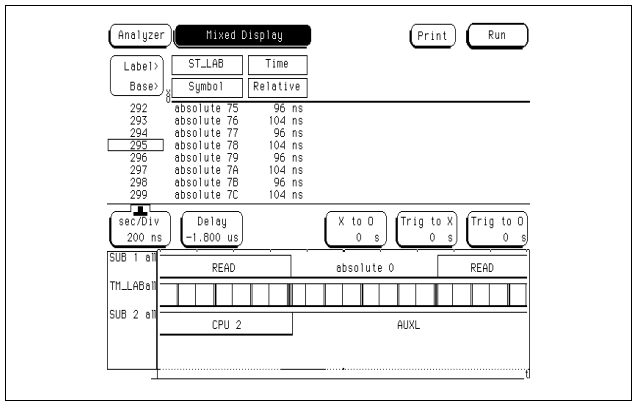
1. Set up a timing and a state analyzer.
2. Go to the state analyzer's Trigger menu.
3. Set Count to Time, and set up the trigger as appropriate.

   You do not need to have one instrument arming the other to display the information jointly, but you do need to turn on Count Time so that the information may be correlated.
4. Set up the timing analyzer trigger.

   Timing analyzers implicitly count time because their sampling is driven by an internal clock, rather than an external state clock.
5. Make a measurement run.
6. Go to the Mixed Display menu.
7. To insert state listings, select any label field from the state listing. From the pop-up that appears, select the desired label to insert.
8. To insert timing waveforms, double-select the label field to the left of the waveform display area. From the pop-up that appears, select insert, and then the appropriate label.

   You can also position X and O Time markers on the waveform display. Once set, the time markers will be displayed in both the listing and the waveform display areas. Note that even if you set X and O Time markers in another display, you must also set the Time markers in the Mixed Display if Time markers are desired.

You can use the Mixed Display feature in the analyzer menu to show both waveforms and trace lists in the same display, making it easier to correlate the events of interest.



Mixed Display using Timing and State in the HP 1661CP

File Management

File Management

Being able to transfer data to a host computer, such as a PC or UNIX workstation, can enhance the logic analyzer in many ways. You can use the host to store configuration files or measurement results for later review. You can save screen images from the logic analyzer in bitmap files to include in reports developed using word processors or desktop publishing tools. Or, you can develop programs on the PC that manipulate measurement results to satisfy your problem-solving needs.

This chapter shows you how to save the different types of information. The examples store files on the flexible disk drive, but you can move the same files to your host computer using a network interface. The HP 1660CP family of logic analyzers have HP-IB and RS-232-C capabilities, and an ethernet interface. If you need help using the LAN interface, see the *LAN User's Guide.*

You can also use a host computer to send the logic analyzer complex command sequences—allowing you to automate your measurement tasks. If you want to program the analyzer using a host computer, see the *HP 1660C/CS/CP-Series Logic Analyzers Programmer's Guide*.

Transferring Files Using the Flexible Disk Drive

Because the flexible disk drive on the HP 1660CP-series logic analyzer will read and write double-sided, double-density, or high-density disks in MS-DOS format, it is a useful tool for transferring data to and from IBM PC-compatible computers as well as transferring data to and from other systems that can read and write MS-DOS format. You can save configuration files, measurement results, and even menu and measurement images from the screen.

This section shows you how to use the flexible disk drive to:

- Save a configuration
- Load a configuration
- Save a trace list in ASCII format
- Save a screen image (such as a display or menu)
- Load additional software

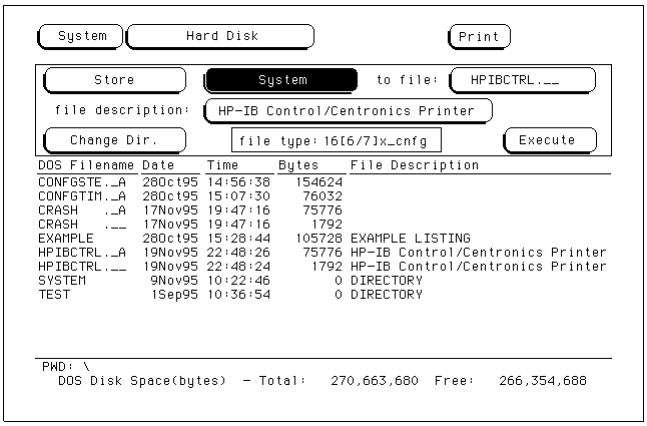
To save a configuration

You can save configurations on a 3.5-inch disk or on the internal hard disk for later use. This is especially useful for automating repetitive measurements for production testing.

1. Go to the System Hard Disk or System Flexible Disk menu.
2. Set the field under System to Store.
3. Select the type of configuration you want to save in the field to the right of Store.

   You can save the analyzer configuration, the system configuration, or both.
4. Specify a file name into which to save the configuration using the to file field.
5. Enter a description for the file using the file description field.
6. Select Execute.

If you want to save your file in a directory other than the root, you can select Change Directory from the disk operations field, then type the name of the desired directory in the directory name field or select it from the list of visible directories using the knob.



Saving the System Configuration for Programmatic Control

To load a configuration

You can quickly load a previously saved configuration, so that you will not have to manually set up the measurement parameters.

1. **Go to the System Hard Disk or System Flexible Disk menu.**

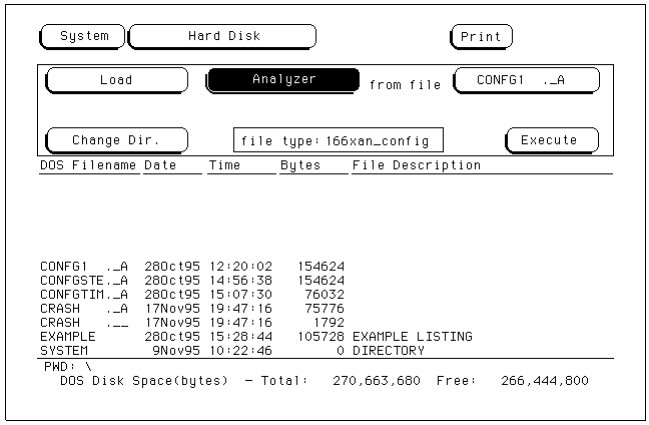
   Your choice here depends on where you saved the configuration.

2. **Select the field below System and select Load from the pop-up menu.**
3. **Select the destination from the module list.**

   "System" loads only settings available under the System menus. "Analyzer" loads data and settings for the analyzer. "All" loads both the system and analyzer configurations.

   You can only load configuration files to the area from which the configuration was taken. For instance, you cannot load an analyzer configuration file to the system. Thus, if you select System, then select a file that contains only an analyzer configuration, the configuration will fail. The file type field tells you what type of information is in a file. Analyzer configuration files show "166xan_config", and system configurations show "16[6/7]x_cnfg" in the file type field.

4. **Specify a file name from which to load the configuration using the from file field or scrolling with the knob.**
5. **Select Execute.**



Loading System Configuration for Programmatic Control

To save a trace list in ASCII format

Some screens, such as file lists and trace lists, contain columns of ASCII data that you may want to move to a computer for further manipulation or analysis. You can save these displays as ASCII files. While a screen capture saves only the data shown onscreen, saving the display as an ASCII file captures all data in the list, even if it is offscreen.

1. Insert a DOS-formatted 3.5-inch disk in the flexible disk drive.
2. Set up the menu you want to capture, or run a measurement from which you want to save data.

   Remember that only displays that present lists of textual data can be captured as ASCII files.
3. Select Print and choose Print Disk from the pop-up menu.
4. Select the Filename field and specify a file name to which the data will be saved.
5. Select ASCII (ALL) from the Output Format field.

   If the current display contents can not be saved as an ASCII file, this option will not be present in the Output Format field.
6. Select Flexible Disk from the Output Disk menu, then select Execute.

```
 68332EVS   -  State Listing


Label     ADDR        CPU32 Mnemonic                          STAT
_________ _____ ____________________________________ ________________

      0    406F4    ANDI.L   #********,(A6)+           Opcode Fetch
      1    0FF7A      0004 data write                  Data Write
      2    0FF7C      06F6 data write                  Data Write
      3    40992    BSR.B    0004093E                 Opcode Fetch
      4    40994 nu MOVE.B   ********,(****,A7)       Opcode Fetch
      5    0FF76      0004 data write                  Data Write
      6    0FF78      0994 data write                  Data Write
      7    4093E    MOVE.W   #03FF,00FFFA46           Opcode Fetch
      8    40940      03FF  pgm read                   Opcode Fetch
      9    40942      00FF  pgm read                   Opcode Fetch
     10    40944      FA46  pgm read                   Opcode Fetch
```

Part of a Trace Listing Saved as an ASCII File

To save a screen's image

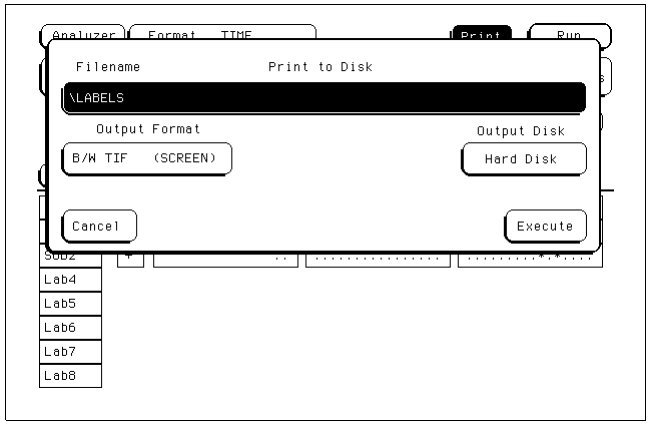
You can save menus and measurements to disk in one of four different graphical formats.

1. Insert a formatted flexible disk in the flexible disk drive.
2. Set up the menu whose image you want to capture, or run a measurement from which you want to save data.
3. Select Print and choose Print Disk from the pop-up menu.

   If the screen contains a pop-up menu, the Print field is not available. Pop-up menus cannot be saved to file unless you are using a controller.
4. Select the Filename field and specify a file name to save to.
5. Select the Output Format field and choose the output format for the graphics file from the pop-up menu.

   Choose one of the following formats:

   - B/W TIF is a black-and-white TIFF (Tagged Image File Format), v 5.0.
   - GRAY TIF is a grayscale TIFF file in TIFF version 5.0 format.
   - PCX is a grayscale PCX file (PCX is the PC Paintbrush and Publisher's Paintbrush format from ZSoft).
   - EPS is a black-and-white Encapsulated PostScript™ file.
6. Select Flexible Disk from the Output Disk menu, then select Execute.



Print Disk Menu

To load additional software

You can enhance the power of your HP 1660CP-series logic analyzer by installing software such as symbol utilities. The software comes with installation instructions. In general, however, you can install logic analyzer software by following these instructions.

1. Turn off the logic analyzer.
2. Insert the first disk of the software into the flexible disk drive.
3. Turn on the logic analyzer.

   The analyzer will load the software as it powers up.
4. To permanently install the software, follow the instructions that come with it.

Reference

Logic Analyzer Description

The HP 1660CP-series logic analyzers are part of a family of general-purpose logic analyzers. The HP 1660CP-series consists of four models ranging in channel width from 34 channels to 136 channels, with 100-MHz state and 500-MHz timing speeds and a 200 M Vector/s pattern generator. The HP 1660CP-series logic analyzers are designed as full-featured standalone or network-configurable instruments for use by digital and microprocessor hardware and software designers. All models have HP-IB, RS-232-C, and Centronics interfaces for hard copy printouts and control by a host computer, and have ethernet LAN interfaces.

Analyzer memory depth is 4 K per channel in all pod pair groupings, or 8 K per channel on one pod of a pod pair (half-channel mode). Pattern generator memory is 258,048 vectors.

Measurement data is displayed as data listings and waveforms, and can also be plotted on a chart or compared to a reference image. Profiled data is displayed as histograms of activity by time, state, or address range.

The 100-MHz state analyzer has master, master/slave, and demultiplexed clocking modes available. Measurement data can be stamped with state or time tags. For triggering and data storage, the state analyzer uses 12 sequence levels with two-way branching, 10 pattern resource terms, 2 range terms, and 2 timers.

The 500-MHz timing analyzer has conventional, transitional, and glitch timing modes with variable width, depth, and speed selections. Sequential triggering uses 10 sequence levels with two-way branching, 10 pattern resource terms, 2 range terms, 2 edge terms and 2 timers.

The 200 M Vector/s pattern generator has a memory depth of 258,048 vectors with a maximum of 32 channels of digital stimulus.

The four analyzer models in the HP 1660CP-series offer a wide variety of channel widths and memory depth combinations. The number of data channels range from 34 channels with the HP 1663CP, to a maximum of 136 channels with the HP 1660CP. In addition, a half-channel acquisition mode is available which doubles memory depth from 4 K to 8 K per channel while reducing channel width by half.

The configuration guide below illustrates the memory depth/channel width combinations in all acquisition modes with all analyzer models.

Table 8-1 **State Analyzer Configurations**

Mode	HP 1660CP	HP 1661CP	HP 1662CP	HP 1663CP
Half-channel 100 MHz	8K-deep / 68 chan. 65 data + 3 data or clock	8K-deep / 51 chan. 48 data + 3 data or clock	8K-deep / 34 chan. 32 data + 2 data or clock	8K-deep / 17 chan. 16 data + 1 data or clock
Full-channel 100 MHz	4K-deep / 136 chan. 130 data + 6 data or clock	4K-deep / 102 chan. 96 data + 6 data or clock	4K-deep / 68 chan. 64 data +4 data or clock	4K-deep / 34 chan. 32 data + 2 data or clock

State Analyzer Configuration Considerations

- Unused clock channels can be used as data channels.
- With Time or State tags turned on, memory depth is reduced by half. However, full depth is retained if you leave one pod pair unassigned.

Table 8-2 **Timing Analyzer Configurations**

Mode	HP 1660CP	HP 1661CP	HP 1662CP	HP 1663CP
Conventional half-channel 500 MHz	8K-deep / 68 chan. 65 data + 3 data or clock	8K-deep / 51 chan. 48 data + 3 data or clock	8K-deep / 34 chan. 32 data + 2 data or clock	8K-deep / 17 chan. 16 data + 1 data or clock
Conventional full-channel 250 MHz	4K-deep / 136 chan. 130 data + 6 data or clock	4K-deep / 102 chan. 96 data + 6 data or clock	4K-deep / 68 chan. 64 data + 4 data or clock	4K-deep / 34 chan. 32 data + 2 data or clock
Transitional half-channel 250 MHz	8K-deep / 68 chan. 65 data + 3 data or clock	8K-deep / 51 chan. 48 data + 3 data or clock	8K-deep / 34 chan. 32 data + 2 data or clock	8K-deep / 17 chan. 16 data + 1 data or clock
Transitional full-channel 125 MHz	4K-deep / 136 chan. 130 data + 6 data or clock	4K-deep / 102 chan. 96 data + 6 data or clock	4K-deep / 68 chan. 64 data + 4 data or clock	4K-deep / 34 chan. 32 data + 2 data or clock
Glitch half-channel 125 MHz	4K-deep / 68 chan. 65 data + 3 data or clock	4K-deep / 51 chan. 48 data + 3 data or clock	4K-deep / 34 chan. 32 data + 2 data or clock	4K-deep / 17 chan. 16 data + 1 data or clock

Timing Analyzer Configuration Considerations

- Unused clock channels can be used as data channels.
- In Glitch half-channel mode, memory is split between data and glitches.

Probing

This section discusses the probing system for the logic analyzer. It also contains the information you need for connecting the probe system components to each other, to the logic analyzer, to the pattern generator, and to the system under test.

Probing Options

You can connect the logic analyzer to your system under test in one of the following ways:

- Microprocessor- and bus-specific interfaces (optional).
- Standard general-purpose probing (provided).
- Direct connection to a 20-pin, 3M-Series type header connector using the optional termination adapter.

See Also *Accessories for HP Logic Analyzers* for additional information about the microprocessor interface kits and for any new probing solutions.

Microprocessor and Bus-Specific Interfaces

There are a number of microprocessor- and bus-specific interfaces available as optional accessories. Microprocessors are supported by Universal Interfaces or Preprocessor Interfaces, or in some cases, both.

Universal Interfaces are manufactured by other vendors. Universal Interfaces are aimed at initial hardware turn-on, and provide fast, reliable, and convenient connections to the microprocessor system. Many use passive probing and do not support inverse assembly.

Preprocessor interfaces are aimed at hardware turn-on and hardware/software integration, and provide the following:

- All clocking and demultiplexing circuits needed to capture the system's operation.
- Additional status lines to further decode the operation of the CPU.
- Inverse assembly software to translate logic levels captured by the logic analyzer into microprocessor mnemonics.

Bus interfaces will support bus analysis for the following:

- Bus support for HP-IB, RS-232-C, RS-449, SCSI, VME, and VXI.

General-Purpose Probing

General-purpose probing connects the logic analyzer probes directly to your target system without using any interface. General-purpose probing does not limit you to specific hookup schemes.

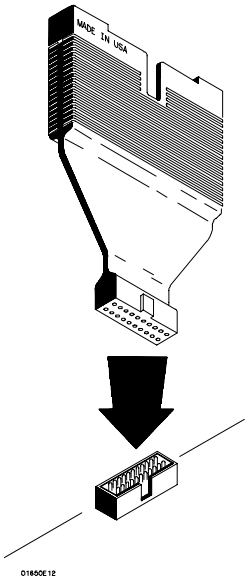
General-purpose probing uses grabbers that connect to both through-hole and surface-mount components. General-purpose probing comes as the standard probing option. You will find a full description of its components and use later in this section.

The Termination Adapter

The logic analyzer must be properly terminated to operate correctly. Most HP preprocessor interfaces have properly terminated state connectors; however, many of them require termination adapters for the timing connectors.

The optional termination adapter lets you connect the logic analyzer probe cables directly to test ports on your target system without the probes.

The termination adapter is designed to connect to a 20-position (2x10), 4-wall, low-profile, header connector which is a 3M-Series 3592 or equivalent.



Termination Adapter

General-purpose probing system description

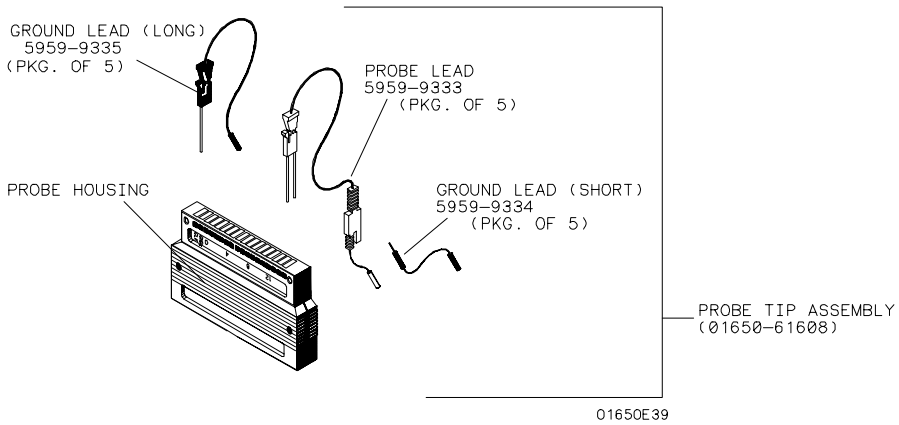
The standard probing system provided with the logic analyzer consists of a probe tip assembly, probe cable, and grabbers. Because of the passive design of the probes, there are no active circuits at the outer end of the cable. The rest of this chapter is dedicated to general-purpose probing.

The passive probing system is similar to the probing system used with high-frequency oscilloscopes. It consists of a series RC network (90 kΩ in parallel with 8 pF) at the probe tip, and a shielded, resistive transmission line. The advantages of this system include the following:

- 250 Ω in series with 8-pF input capacitance at the probe tip for minimal loading
- Signal ground at the probe tip for high-speed timing signals
- Inexpensive, removable probe tip assemblies

Probe Tip Assemblies

Probe tip assemblies lets you connect the logic analyzer directly to the target system. This general-purpose probing is useful for discrete digital circuits. Each probe tip assembly contains 16 probe leads (data channels), 1 clock lead, a pod ground lead, and a ground tap for each of the 16 probe leads.



Probe Tip Assembly

Probe and Pod Grounding

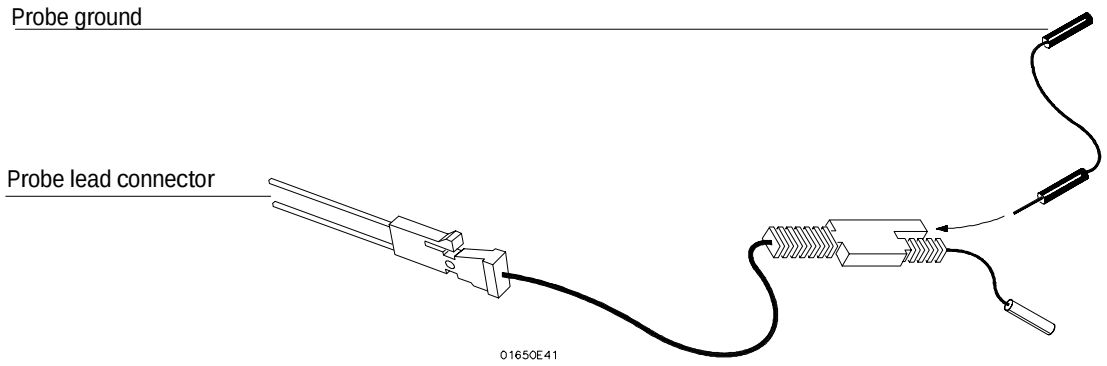
Each pod is grounded by a long, black, pod ground lead. You can connect the ground lead directly to a ground pin on your target system or use a grabber. To connect the ground lead to grounded pins on your target system, you must use 0.63-mm (0.025-in) square pins, or use round pins with a diameter of 0.66 mm (0.026 in) to 0.84 mm (0.033 in). The pod ground lead must always be used.

Each probe can be individually grounded with a short black extension lead that connects to the probe tip socket. You can then use a grabber or the grounded pins on your target system in the same way you connect the data lines. For extra confidence in your measurements, grounding every third or fourth probe is recommended.

When probing signals with rise and fall times of 1 ns or less, grounding each probe lead with the 2-inch ground lead is recommended. In addition, always use the probe ground on a clock probe.

Probe Leads

The probe leads consists of one 12-inch twisted-pair cable, one ground tap, and one grabber. The probe lead, which connects to the target system, has an integrated RC network with an input impedance of 100 kΩ in parallel with approximately 8 pF, and all in series with 250 Ω. The probe lead has a two-pin connector on one end that snaps into the probe housing.



Probe Ground Lead

Grabbers

The grabbers have a small hook that fits around the IC pins and component leads. The grabbers have been designed to fit on adjacent IC pins on either through-hole or surface-mount components with lead spacing greater than or equal to 0.050 inches.

Probe Cable

The probe cable contains 18 signal lines, 17 chassis ground lines and two power lines for preprocessor use. The cables are woven together into a flat ribbon that is 4.5 feet long. The probe cable connects the logic analyzer to the pods, termination adapter, or preprocessor. Each cable is capable of carrying 0.33 amps for preprocessor power.

CAUTION DO NOT exceed 0.33 amps per cable, or the cable will be damaged.

Preprocessor power is protected by a current limiting circuit. If the current limiting circuit is activated, the fault condition must be removed. After the fault condition is removed, the circuit will reset in one minute.

Minimum Signal Amplitude

Any signal line you intend to probe with the logic analyzer probes must supply a minimum voltage swing of 500 mV to the probe tip. If you measure signal lines with a voltage swing of less than 500 mV, you may not obtain a reliable measurement. Because the minimum input overdrive is the greater of 250 mV or 30% of input amplitude, be sure to correctly set the pod threshold in the Analyzer Format menu.

Maximum Probe Input Voltage

The maximum input voltage of each logic analyzer probe is 40 volts peak.

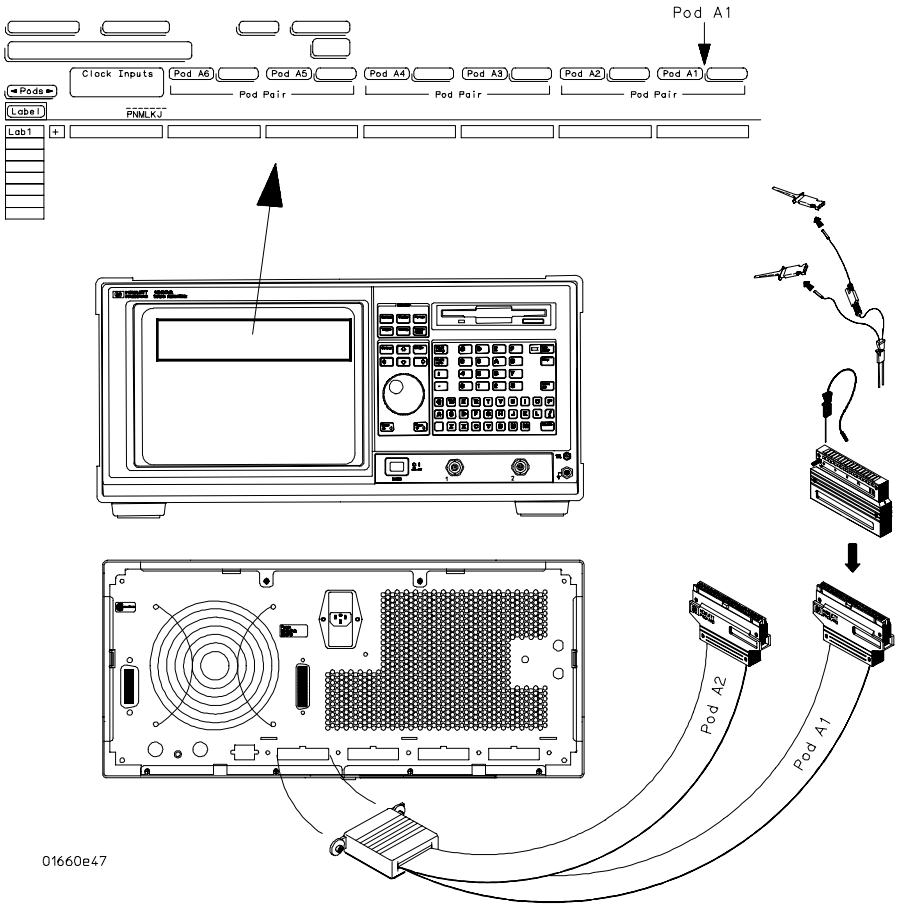
Pod Thresholds

Logic analyzer pods have two preset thresholds and a user-definable pod threshold. The two preset thresholds are ECL (–1.3 V) and TTL (+1.5 V). The user-definable threshold can be set anywhere between –6.0 volts and +6.0 volts in 0.05 volt increments.

All pod thresholds are set independently.

Assembling the probing system

The general-purpose probing system components are assembled as shown to make a connection between the measured signal line and the pods displayed in the Analyzer Format menu.



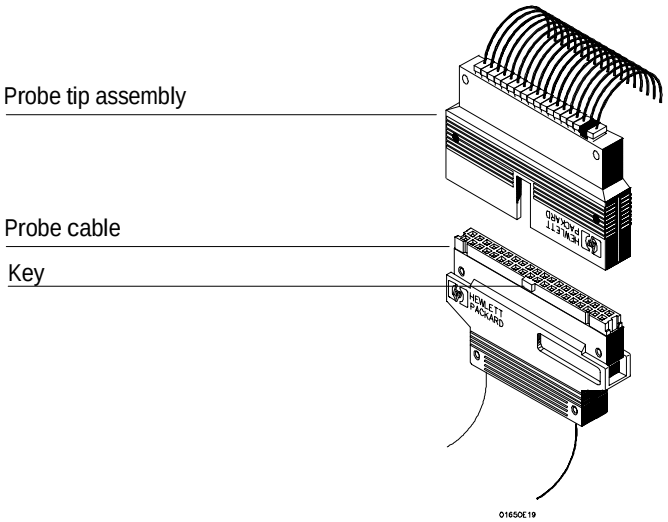
Connecting Probe Cables to the Logic Analyzer

Connecting Probe Cables to the Logic Analyzer

All probe cables are installed at Hewlett-Packard. If you need to replace a probe cable, refer to the *HP 1660C/CS/CP-Series Logic Analyzers Service Guide*. You can purchase the Service Guide from your HP Sales Office.

Connecting the Probe Tip Assembly to the Probe Cable

To connect a probe tip assembly to a cable, align the key on the cable connector with the slot on the probe housing and press them together.



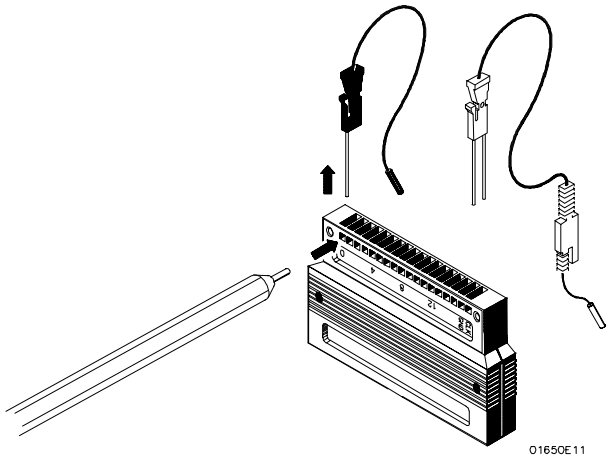
Connecting Probe Tip Assembly

Disconnecting Probe Leads from Probe Tip Assemblies

When you receive the logic analyzer, the probe leads are already installed in the probe tip assemblies. To keep unused probe leads out of your way during a measurement, you can disconnect them from the pod.

To disconnect a probe lead, insert the tip of a ballpoint pen into the latch opening. Push on the latch while gently pulling the probe out of the pod connector as shown in the figure.

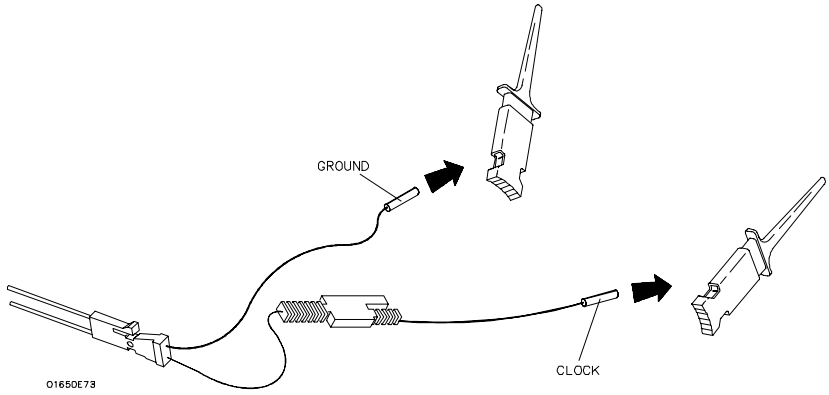
To connect the probes into the pods, insert the double pin end of the probe into the probe housing. Both the double pin end of the probe and the probe housing are keyed so they will fit together only one way.



Installing Probe Leads

Connecting the Grabbers to the Probes

Connect the grabbers to the probe leads by slipping the connector at the end of the probe onto the recessed pin located in the side of the grabber. If you need to use grabbers for either the pod or the probe grounds, connect the grabbers to the ground leads in the same manner.



Connecting Grabbers to Probes

Keyboard Shortcuts

This section explains how to use the optional keyboard interface (HP E2427B Keyboard Kit). You can use the keyboard interchangeably with the knob and front-panel keypad for all menu applications. The keyboard functions fall into the two basic categories of cursor movement and data entry.

Moving the cursor

The keyboard cursor is the location on the screen highlighted in inverse video. Move the cursor using one of the methods described below.

Keyboard cursor movement

There are four cursor keys marked with arrows on the keyboard. These keys act as follows:

- Up-pointing arrow moves the cursor up.
- Down-pointing arrow moves the cursor down.
- Right-pointing arrow moves the cursor to the right.
- Left-pointing arrow moves the cursor to the left.

The cursor keys do not wrap. This means that pressing the right-pointing arrow when the cursor is already at the rightmost point in a menu will have no effect. The cursor keys do repeat, so holding the key down is the fastest way to continue keyboard cursor movement in a given direction.

Page Up and Page Down keys The Page Up and Page Down keys page through listings. The Page Up key displays the previous page of data. The Page Down key displays the next page of data.

Selecting a menu item

To select a menu item with the keyboard, position the cursor (the location highlighted in inverse video) on the menu item and press the Return or Enter key.

Entering data into a menu

When an assignment field is selected, the cursor is displayed under the leftmost character in the field. When you type a character, it is displayed in the cursor position, and the cursor is advanced. Cursor keys move the cursor within the assignment field. Pressing either the Return key or the Enter key will terminate data entry for that item.

Using the keyboard overlays

A keyboard overlay is included in the HP E2427B Keyboard Kit. The table below represents the key mappings.

Key	Functions Like	Key	Functions Like
F1	System Key	S	Select "seconds"
F2	Config Key	M	Select "milliseconds" or "millivolts"
F3	Format Key	U	Select "microseconds"
F4	Trigger Key	N	Select "nanoseconds"
F5	Listing Key	V	Select "volts"
F6	Waveform Key	B	Select "any (both) edge"
F7	Print All Key	R	Select "rising edge"
F8	Run Rep. Key	F	Select "falling edge"
F9	Stop	*	Assign glitch
F10	Done	.	Assign Don't Care (X)
F12	Assign Don't Care (X)		

Common Menu Fields

There are a number of fields that appear throughout the different menus that have similar operation. These common fields are listed below:

- Mode (System/Analyzer) field
- Menu field
- Print field
- Run field
- Base field
- Label field
- Roll fields

Because most of these fields are self-explanatory, only the fields with less obvious features are described here.

Print field

The Print field prints what is displayed on the screen at the time you initiate the printout. When you select the Print field, a print selection pop-up appears showing you one or more of the following options:

- Print Screen
- Print Disk
- Print All
- Print Partial
- Cancel

While printing, the Print field changes to Cancel and the user interface is not active except for Cancel. When the printout is complete, the user interface becomes active again. The Print field is not available with pop-up menus. The only way to print a pop-up menu to disk is with a controller.

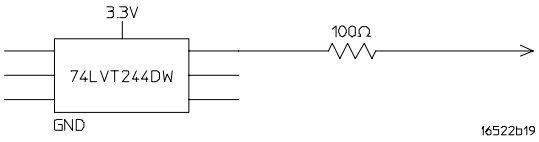
Print Screen

The Print Screen option sends the screen immediately to the specified printer. The option does not create a file; to do that, use Print Disk.

Print Disk

The Print Disk option copies the screen in graphical form or ASCII, if available, to a file on either drive. Possible output formats are

- ASCII 8-bit standard ASCII text file
- B/W TIF Black-and-white image in TIFF version 5.0 format
- GRAY TIF Grayscale image in TIFF version 5.0 format
- PCX Grayscale image in standard PCX format
- EPS Line image in standard Encapsulated PostScript format



Print All

The Print All option prints not only what is displayed on the screen, but data that is below the screen. This option is only available when an ASCII form of the screen is possible. For example, Print All is never available in Waveform.

When you select Print All with a Listing menu, make sure the first line you want to print is in the state location box (also referred to as the data roll field) at the center of the listing area. Lines above this box will not print.

Print Partial

The Print Partial option is identical to the Print All option, except the start and end states are specified. The screen settings and specified data are printed in ASCII form.

Run/Stop field

The Run field starts the analyzer measurement. When you select Run, the screen switches to the display menu last viewed and displays the acquired data. If Stop is selected during a single run, the data acquisition is aborted. If Stop is selected during a repetitive run, the current run cycle is completed before data is displayed.

Repetitive

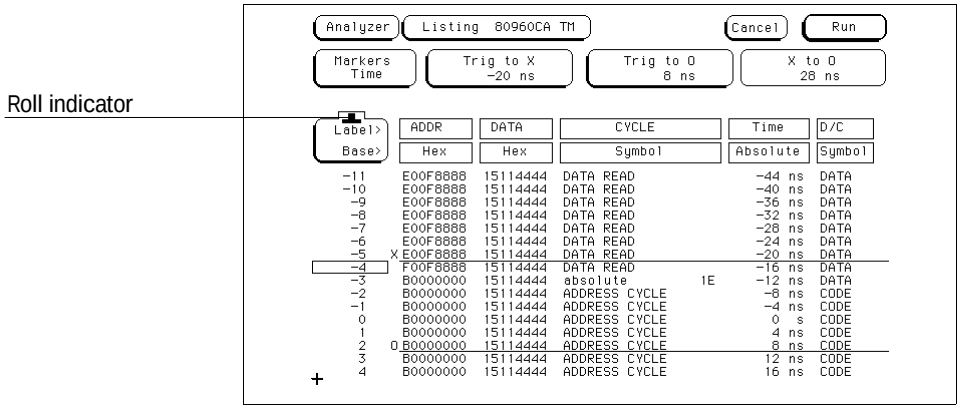
The Repetitive option runs the data acquisition cycle repeatedly until you select Stop or until a pre-assigned stop measurement condition is met. The stop measurement condition is set in the Analyzer Listing or Analyzer Waveform menus when pattern markers are turned on.

Roll fields

Some data may not fit on screen when there are many pods or labels to display. When this happens, it is indicated by the Label/Base field becoming selectable and its shade changing to the common field shade. To move through the hidden data, select the field, wait for the roll indicator to appear, and then use the knob to move through the data. The figure on this page shows an active roll field.

If there is more than one rollable field, the roll indicator remains with the last rollable field activated. For example, the Listing menu shown below has both the Label/Base field and the state location field, which are both rollable. However, the only field affected when turning the knob is the field with the roll indicator.

Another way to move through data is by using the Page keys. The Page keys are independent of the knob rolling function and move through data without changing which labels or pods are displayed. Page keys page data up or down one screen at a time. To move data left or right one screen at a time, press the blue Shift key and then a Page key.



Label and Base Roll Field

Disk Drive Operations

The logic analyzer has a built-in 3.5-inch, double-sided, high-density or double-density, flexible disk drive. The disk drive is compatible with both LIF (Logical Interchange Format) and DOS (Disk Operating System) formats. It also has an internal hard disk drive, which performs the same operations as the flexible disk drive.

Disk operations

Ten disk operations are available:

- Autoload

Designates a set of configuration files to be loaded automatically the next time the analyzer is turned on.

- Copy

Copies files. Any file can be copied from one drive to another, from one directory to another, or to different flexible disks.

- Duplicate Disk

Copies one flexible disk to another flexible disk. You cannot copy the hard disk to a flexible disk in a single operation. All volume labels, directories, and file positions from one disk are copied exactly to another disk. The new disk is formatted to match the source disk if it is required. All files on the destination disk will be destroyed with this operation.

- Format Disk

Formats a flexible disk or the internal hard disk. Either can be formatted in LIF or DOS format. All files on the disk will be destroyed with this operation.

- Load

Loads a file into the logic analyzer, overwriting the current settings or information. You can load system configurations, analyzer measurement setups including measurement data, and inverse assembler files.

- Make Directory

Creates a new directory on a DOS disk. You can save or copy files to the new directory using the store and copy commands. This is not available with LIF disks.

- Pack Disk

Removes all empty or unused sectors between files on a LIF disk so that more space is available. If you select Pack Disk while a DOS disk is in the drive, nothing happens.

- Purge

Purges (deletes) the file you indicate. Deleted files cannot be recovered.

- Rename

Changes the name of the file you select.

- Store

Saves system and analyzer measurement setups including data.

Disk operation safeguards

If there is a problem or additional information is needed to execute an operation, a pop-up appears near the center of the screen displaying the status of the operation.

If executing a disk operation could destroy or damage a file, a pop-up appears when you select Execute. If you do not want to complete the operation, select Cancel to cancel the operation. Otherwise, select Continue.

Autoload

The Autoload operation allows you to designate a set of configuration files to be loaded automatically the next time the analyzer is turned on. This allows you to change the default configuration of certain features to one that better fits your needs. If both the hard drive and flexible drive have autoload setups, only the setup on the flexible drive will be used.

Autoload loads all of the files for a given base filename. If you want to load only one type of file, rename that file or copy it to a separate name and enable it as the current Autoload file. As long as Autoload is enabled before the instrument is shut off, Autoload will remain enabled when you turn on the instrument and load the configuration files.

Format

CAUTION

Executing Format Disk permanently erases all existing information from the disk. After formatting, there is no way to retrieve the original information.

The logic analyzer recognizes a variety of sector sizes for LIF disks. However, it only creates 1024-byte sectors when formatting a LIF disk. DOS disks always have 512-byte sectors.

The logic analyzer does not support track sparing during formatting. If a bad track is found, the disk is considered bad. If a disk has been formatted elsewhere with track sparing, it will be read successfully.

When formatting a disk, the DISK ERROR message appears if the disk is unformatted. This is normal, and you can safely continue the format process.

Pack

By purging files from the disk and adding other files, you may end up with blank areas on the disk (between files) that are too small for the new files you are creating. On LIF disks, the Pack Disk operation packs the current files together, removing unused areas from between the files so that more space is available for files at the end of the disk. On DOS disks, the Pack Disk operation is not available. If you do select Pack Disk while a DOS disk is in the drive, the disk is not affected.

Load and Store

When you choose Load or Store, you next need to set the field immediately to the right. This field presents at least three choices: All, System, and Analyzer. If you have other software loaded, it might add to the list of choices.

All

Choose All to store or load both system and analyzer information. If you are storing, two files (one for the system and one for the analyzer) are created. The system file ends in "._ _" and the analyzer file ends in "._A".

System

System files store system configurations. System information for the HP 1660CP-series consists of settings for printer, controller, RS-232-C, HP-IB, shade, and sound. LAN settings are not saved. System configuration files end in two underscores and have a file type of 16[6/7]x_cnfg.

Analyzer

Analyzer configuration files store measurement setups, including data. If you are storing the current measurement and an inverse assembler is already loaded, when you reload the file you are now creating it will try to pull in the inverse assembler. Other attributes stored in analyzer configuration files include labels, trigger sequence, arming configuration, measurement data, markers, analyzer names, and pod assignments. Analyzer configuration files end in "._A" and have a file type of 166xan_config.

Pattern Generator

Pattern generator files store the configuration attributes and parameters of the pattern generator, including vectors and macros, labels, pod assignments, and clock frequency. Pattern generator configuration files end in "._B" and have a file type of 16522_config.

This section describes the controller and printer interfaces and their configurations found in the System External I/O menu. It defines the HP-IB interface and describes how to select a different HP-IB address. It also defines the RS-232-C interface and tells you how to select a baud rate, how to change the stop bits, how to set the parity and data bits, and how to change the protocol. The Centronics (parallel) interface (for printers only) is also described.

Controller interface

The logic analyzer is equipped with a standard RS-232-C interface and an HP-IB interface that allow you to connect to a controller. Either interface gives you remote access for running measurements, for uploading and downloading configurations and data, and connecting to printers. If you purchased the optional Ethernet LAN interface, it can also be used for controlling the logic analyzer.

Printer interface

The logic analyzer can output its screen to various HP-IB, RS-232-C, and Centronics graphics printers. Configured menus, as well as waveforms and other data, can be printed for complete measurement documentation. Even with the optional Ethernet LAN interface installed, the analyzer cannot use a networked or shared printer.

See Also

Chapter 2, "Connecting Peripherals" for more details on physically connecting equipment.

HP 1660C/CS/CP-Series Logic Analyzers Programmer's Guide for more information on the controller interface.

The *LAN User's Guide* more information on the LAN interface.

The HP-IB interface

The Hewlett-Packard Interface Bus (HP-IB) is Hewlett-Packard's implementation of IEEE Standard 488-1978, "Standard Digital Interface for Programmable Instrumentation." HP-IB is a carefully defined interface that simplifies the integration of various instruments and computers into systems.

The HP-IB interface uses an addressing technique to ensure that each device on the bus (interconnected by HP-IB cables) receives only the data intended for it. To accomplish this, each device is set to a different address and this address is used to communicate with other devices on the bus. The HP-IB address is the only HP-IB interface setting configurable from the logic analyzer.

The HP-IB address can be set to 31 different HP-IB addresses, from 0 to 30. Simply choose a compatible address for your device and software. The default address for all HP logic analyzers is 7. In the System External I/O menu, select HP-IB Settings and then set the Address field to your address.

The RS-232-C interface

The RS-232-C interface is Hewlett-Packard's implementation of EIA Recommended Standard RS-232-C, "Interface Between Data Terminal Equipment and Data Communications Equipment Employing Serial Binary Data Interchange."

With this interface, data is sent one bit at a time and characters are not synchronized with preceding or subsequent data characters. Each character is sent as a complete entity independent of other events.

The paragraphs below describe the settings for RS-232-C. You can change these settings by going to the System External I/O menu and selecting RS232 Settings. Each field in the Settings pop-up menu presents a list of valid choices.

Baud rate

The baud rate is the rate at which bits are transferred between the interface and the peripheral. The baud rate must be set to transmit and receive at the same rate as the peripheral.

Stop Bits

Stop Bits are used to identify the end of a character. The number of Stop Bits must be the same for the controller as for the logic analyzer.

Parity

The parity bit detects errors as incoming characters are received. If the parity bit does not match the expected value, the character was incorrectly received. The action taken when an error is detected depends on the interface and the device program configuration.

Parity is determined by the requirements of the system. The parity bit may be included or omitted from each character by enabling or disabling the parity function.

Data Bits

Data Bits are the number of bits used to represent the binary code of a character. The HP 1660CP-series logic analyzers support 8-bit binary code.

Protocol

Protocol governs the flow of data between the instrument and the external device. It can be controlled either by the hardware, in which case you select None in the RS-232-C Settings pop-up, or by the software, in which case you select Xon/Xoff. Xon/Xoff stands for Transmit On/Transmit Off.

With less than a 5-wire interface, selecting None does not allow the sending or receiving device to control how fast the data is being sent, increasing the possibility of missing data. With a full 5-wire interface, selecting None allows a hardware handshake to occur. With a hardware handshake, hardware signals control data flow. The HP 13242G cable allows the logic analyzer to support hardware handshake.

The Centronics interface

The Centronics interface is an industry-standard parallel printer interface. It can only be used as a printer interface, and is not available to the controller. There are no Centronics-specific settings; page and line length are set in the Printer Settings menu.

See Also

Chapter 2, "Connecting Peripherals," for more information on setting up the parallel printer port.

System Utilities

The System Utilities menu is used for setting system level parameters such as the system clock, display intensity for each shade, and the sound. In this menu you can also rewrite the analyzer's memory with any new revisions of the operating system.

Real Time Clock Adjustments field

A real-time clock is displayed in the Waveform and Listing menus. When you print a screen, the current clock and date appear on the hard copy. To change the clock, go to the System Utilities menu and select Real Time Clock Adjustments. Set the values to the desired date and time. Default Time sets the real time clock to January 1, 1992 at 12 noon.

If your logic analyzer has the optional LAN interface, you will also see a Time Zone field. The Time Zone field changes the logic analyzer's apparent file times when viewed over NFS. It does not affect the real-time clock. Set the Time Zone to the same Time Zone used by your LAN. This value is usually the same as the difference in hours between your local time and Greenwich Mean Time.

Update FLASH ROM field

The logic analyzer uses flash ROMs to store the operating system. The analyzer you received should have an operating system in place and should also include the operating system files on a flexible disk, but you may occasionally need to update the operating system. Update FLASH ROM updates the analyzer's operating system.

CAUTION

Updating flash ROM without the proper files will damage the logic analyzer operating system.

1. Go to the System Utilities menu.
2. Select Update FLASH ROM.

The analyzer warns, "Selecting Continue Will Erase & Update Flash ROMs." and waits for you to select Cancel or Continue. If you select Continue, the analyzer will be reset. If you need to save the measurement data, select Cancel.

3 Select Continue.

The screen goes black and the analyzer performs its power-up self tests. It then displays a message listing the required files and provides further instructions.

4 Insert the update disk into the flexible disk drive.

5 To search only the flexible disk drive, press the Done key. To search the flexible disk drive and then the hard drive, press any other key.

If you press a key other than Done, the logic analyzer will not pause for you to insert the second disk when it finishes copying files from the first disk. Instead, it will look on the hard drive under the /SYSTEM directory. If it finds copies of the operating system files on the hard drive, those are used instead. This could result in incorrect installation of the updated operating system.

The logic analyzer warns, "We are about to erase flash ROM memory." This is the last point at which you can cancel the operation. Any loss of power between the time the analyzer starts to erase flash ROM and the time it finishes copying the update will destroy the operating system.

CAUTION

If you do not have the required files, turn off the analyzer immediately. Pressing any key will destroy the operating system.

6 If you are sure you are ready to continue, press any key.

7 When the analyzer has completed the update, press any key.

The screen goes black and the analyzer reboots. You have finished updating the flash ROM and the new operating system is in place. It is now safe to turn off the logic analyzer.

Shade adjustments

You can adjust the greys of the display to different levels of intensity. Select the shade number, then select luminosity and adjust it with the knob. Default Shades restores all shade intensity levels to the original factory settings.

Type field

The Type field lets you configure the logic analyzer with either an internal clock (Timing mode) or an external clock (State and SPA). When the Type field is selected, the following choices are available.

Timing

When Timing is selected, the analyzer uses its own internal clock to clock measurement data into the acquisition memory. This clock is asynchronous to the signals in the target system. Fields relating to external clocks such as the Analyzer Format menu's Master Clock do not appear and certain menus such as Compare are not available.

The analyzer can only be configured with one timing analyzer. If two are selected, the first will be turned off.

State

When State is selected, the analyzer uses a clock from the system under test to clock measurement data into acquisition memory. This clock is synchronous to the signals in the target system.

SPA

SPA stands for System Performance Analysis. It uses an external clock like a state analyzer but measures overall system performance rather than recording discrete activity. For more details on SPA, see Chapter 9.

Illegal configuration

When both analyzers are turned on, the first pod pair 1,2 and the last pod pair (5,6 in the 96-channel model or 7,8 in the 128-channel model) cannot be assigned to the same analyzer machine. If this configuration is set, the analyzer will display a re-assignment menu when you try to leave the configuration screen. Use this re-assignment menu to configure the pod assignment automatically to a legal configuration.

The Analyzer Format Menu

Pod threshold field

The pod threshold field is used to set a voltage level that the data must reach before the analyzer recognizes and displays it as a change in logic levels. Threshold levels apply to single pods, and cover both data and clock channels.

TTL When TTL is selected as the threshold level, the data signals must reach +1.5 volts.

ECL When ECL is selected as the threshold level, the data signals must reach –1.3 volts.

User When User is selected as the threshold level, the data signals must reach a user selectable value. The range of this value is between –6.0 volts to +6.0 volts in 50-mV increments.

State acquisition modes (state only)

The State Acquisition Mode field identifies the channel width and memory depth of the selected acquisition mode. There are two configurations of channel width/memory depth.

Full Channel/4K Memory/100 MHz

Full-channel mode uses both pods in a pod pair for 34 channels of width and a total memory depth of 4 K per channel. If time or state tags are turned on, the total memory is evenly split between data acquisition storage and time or state tag storage. To maintain the full 4 K per channel depth with state or time tags, leave one pod pair unassigned.

Half Channel/8K Memory/100 MHz

Half-channel mode cuts the channel width to 17 channels. In this mode, the pod used within the pod pair is selected through the Pod field. In half-channel mode, the memory depth is increased to 8 K per channel. Time or state tags are not available in this mode.

Timing acquisition modes (timing only)

The Timing Acquisition mode field identifies the acquisition type, the channel width, and sampling speed of the present acquisition mode. There are three acquisition modes and five configurations.

Conventional Acquisition Mode

In Conventional Acquisition mode, the analyzer stores measurement data at each sampling interval.

Conventional full-channel 250 MHz The total memory depth is 4 K with data being sampled and stored as often as every 4 ns.

Conventional half-channel 500 MHz The total memory depth is 8 K with data being sampled and stored as often as every 2 ns.

Transitional Acquisition Mode

In Transitional Acquisition mode the timing analyzer samples data at regular intervals, but it only stores the data when it detects a transition on some channel. Both transitional modes store time tags for each stored data sample.

Transitional full-channel 125 MHz The total memory depth is 4 K per channel with 34 channels per pod pair. Data is sampled for new transitions as often as every 8 ns.

Transitional half-channel 250 MHz The total memory depth is 8 K with 17 channels on one pod. The pod used within the pod pair is selectable. Data is sampled for new transitions as often as every 4 ns.

Glitch Acquisition Mode

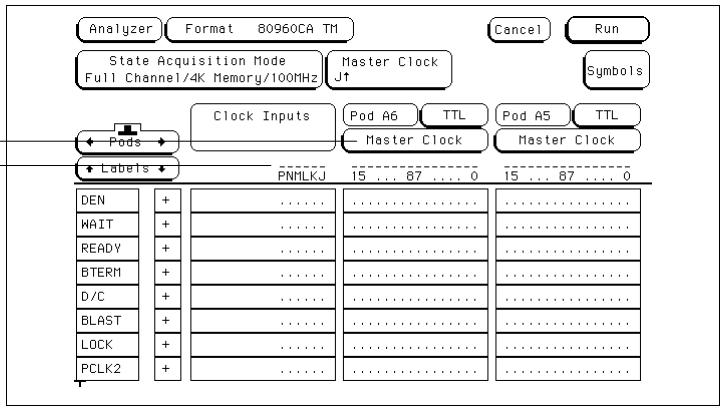
A glitch is defined as a pulse with a minimum width of 3.5 ns and a maximum width of the sample period. In Glitch Acquisition mode, the timing analyzer samples data at regular intervals as it does in Conventional Acquisition mode, but it also looks for a rising and a falling edge occurring between samples. Every sample is stored. When an edge pair is detected in the sample period, a vertical dashed line is displayed.

Glitch half-channel 125 MHz In Glitch mode, the total memory depth is split between data storage and glitch storage. Data acquisition memory depth is 2 K per channel. Glitch storage is 2 K per channel. Data is sampled for new transitions every 8 ns, or with every sample period if it is larger.

Clock Inputs Display

Beneath the Clock Inputs display, and next to the activity indicators, is a group of all clock inputs available in the present configuration. The number of available clocks depends on the model. The J and K clocks appear with pod pair 1/2, the L and M with pod pair 3/4, and N and P with pod pairs 7/8 for the HP 1660 and 5/6 for the HP 1661. In a model with more than three pod pairs, all other clock lines are displayed to the left of the displayed master clocks, and are used only as data channels.

With the exception of the Range resource, all unused clock bits can be used as data channels in the trigger terms. Activity indicators above the clock identifier show clock or data signal activity.



Pod Clocks

Pod clock field (State only)

The pod clock field identifies the type of clock arrangement assigned to each pod. When the pod clock field is selected, a clock arrangement menu appears with the choices of Master, Slave, or Demultiplex. Once a pod clock is assigned a clock arrangement, its identity and function follows what is configured in the Master and Slave Clock fields.

Master

This option specifies that data on all pods designated "Master Clock," in the same analyzer, are strobed into memory when the status of the clock lines match the clocking arrangement specified under the Master Clock.

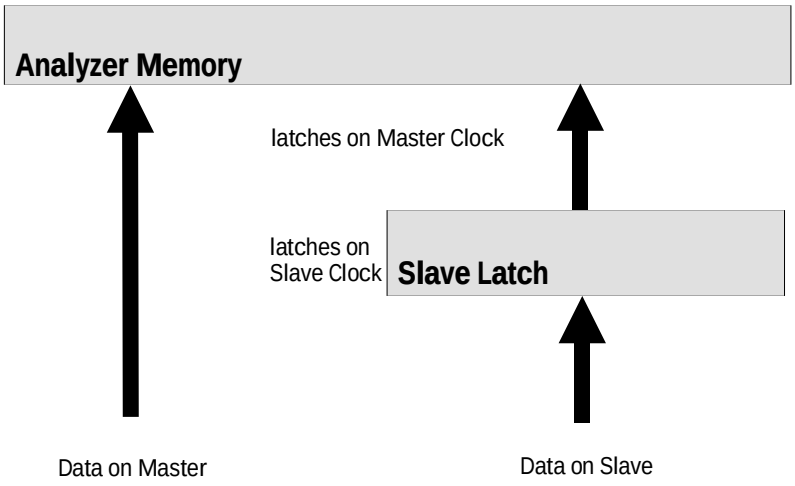
See Also

"Master and Slave Clock fields (State only)" found later in this section for information about configuring a clocking arrangement.

Slave

This option specifies that data on a pod designated "Slave Clock" is latched when the status of the slave clock meets the requirements of the slave clocking arrangement. Then, followed by a match of the master clock and the master clock arrangement, the slave data is strobed into analyzer memory along with the master data. See the figure below.

If multiple slave clocks occur between master clocks, only the data latched by the last slave clock prior to the master clock is strobed into analyzer memory.



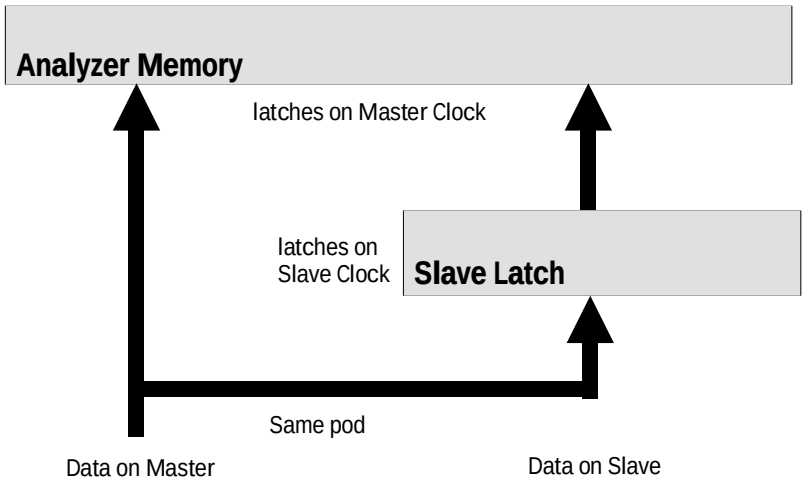
Latching Slave Data

Demultiplex

The Demultiplex mode is used to store two different sets of data that occur at different times on the same channels. In Demultiplex mode both the master and slave clocks are used, but only one pod of the pod pair is sampled.

Channel assignments are displayed as Demux Master and Demux Slave. For easy recognition of the two sets of data, assign slave and master data to separate labels.

When the analyzer sees a match between the slave clock input and the Slave Clock arrangement, Demux Slave data is latched. Then, followed by a match of the master clock and the master clock arrangement, the slave data is strobed into analyzer memory along with the master data. If multiple slave clocks occur between master clocks, only the most recently latched data is strobed into analyzer memory.



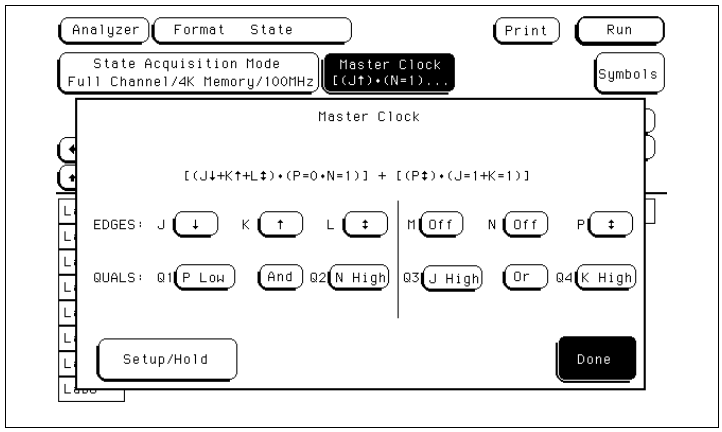
Latching Slave Data in Demultiplex Mode

Master and Slave Clock fields (State only)

The Master and Slave Clock fields are used to construct a clocking arrangement. A clocking arrangement is the assignment of appropriate clocks, clock edges, and clock qualifier levels which allow the analyzer to synchronize itself on valid data.

Clock selections

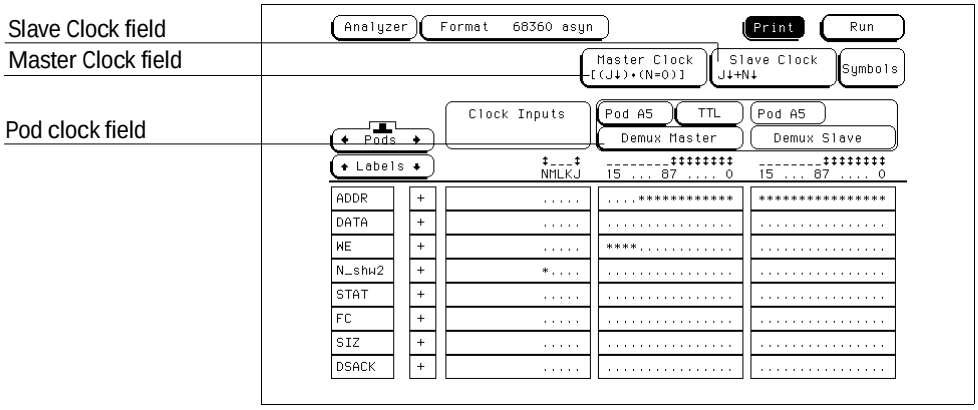
When the Master or Slave Clock field is selected, a clock/qualifier selection menu appears showing the available clocks and qualifiers for a clocking arrangement. Depending on the model, there are a maximum of six clocks available (J through P), and a maximum of four clock qualifiers available (Q1 through Q4).



Clock/Qualifier Selection Menu

Clock edges are ORed to clock edges, clock qualifiers are ANDed to clock edges, and clock qualifiers can be either ANDed or ORed together. All clock and qualifier combinations on the left side of the graphic line are ORed to all combinations on the right side of the line. For example, in a six-clock model, all combinations of the J, K, and L clock with Q1 and Q2 qualifiers, are ORed to the clock combinations of the M, N, and P clocks with Q3 and Q4 qualifiers.

See Also "Pod Clock Field" found earlier in this chapter for information on selecting clocking arrangement types, such as Master, Slave, or Demultiplex.



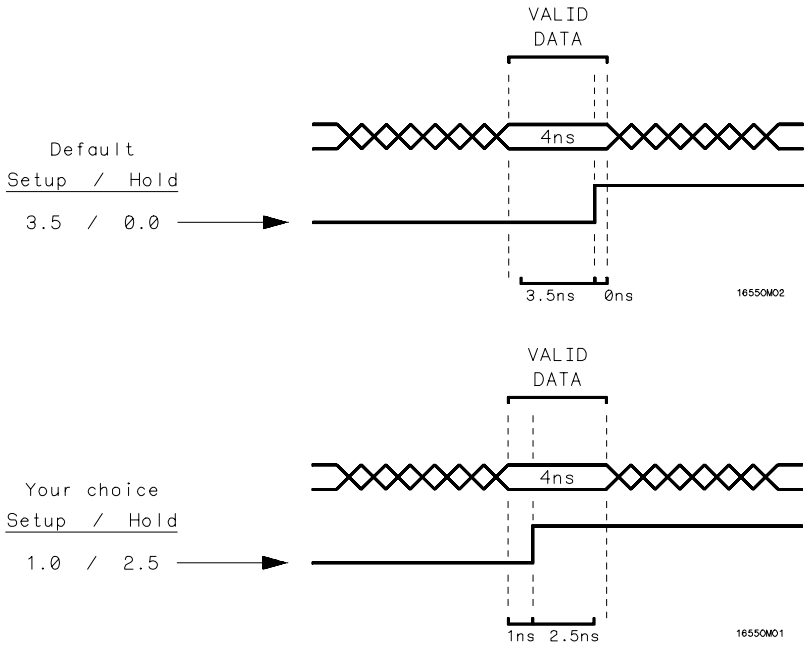
Clock Fields

Setup/Hold field

Setup/Hold in the Master and Slave Clock fields adjusts the relative position of the clock edge with respect to the time period that data is valid. When the Setup/Hold field is selected, a configuration menu appears. Use this Setup/Hold configuration menu to select each pod in the analyzer and assign a Setup/Hold selection from the selection list.

With a single clock edge assigned, the choices range from 3.5-ns Setup/0.0-ns Hold to 0.0-ns Setup/3.5-ns Hold. With both edges of a single clock assigned, the choices are from 4.0-ns Setup/0.0-ns Hold to 0.0-ns Setup/4.0-ns Hold. If the analyzer has multiple clock edges assigned, the choices range from 4.5-ns Setup/0.0-ns Hold to 0.0-ns Setup/4.5-ns Hold.

The relationship of the clock signal and valid data under the default setup and hold is shown in the upper figure. If the relationship of the clock signal and valid data is such that the data is valid for 1 ns before the clock occurs and 3 ns after the clock occurs, you will want to use the 1.0 setup and 2.5 hold setting as shown in the lower figure.



Clock Position in Valid Data

Symbols field

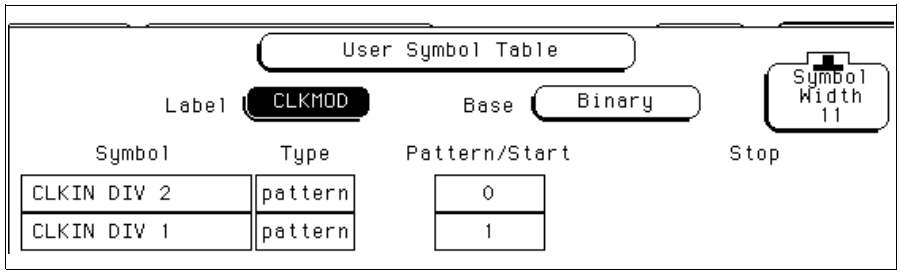
The Symbols field is located directly below the Run field in the upper right corner of the Format menu. Use this field to access the symbol tables.

Use symbol tables to define a mnemonic for a specific bit pattern of a label. You can specify up to 1000 total symbols, and use them freely between available analyzers. When measurements are made, the mnemonic is displayed where the bit pattern occurs using the selected symbol base. You can also download compiled symbol tables using HP E2450A Symbol Utility, which is supplied with the logic analyzer.

See Also *HP E2450A Symbol Utility User's Guide* for more information on downloading symbols.

Label field

The Label field identifies the label for which you are specifying symbols. When you select this field, a selection menu appears that lists all the labels turned on for that analyzer. Each label has a separate symbol table, so you can give the same name to symbols defined under different labels.



Symbol Pop-up Menu

Base field

Use the Base field to select the numeric base in which the pattern in the symbols menu is displayed. Binary is not available if more than 20 channels are assigned to a label because there is only enough room for 20 bits to be displayed on the screen.

You cannot specify a pattern or range when the base is ASCII. Define the pattern or range in one of the other bases, then switch to ASCII to see the ASCII characters.

Symbol Width field

The Symbol Width field specifies how many characters of the symbol name will be displayed when the symbol is referenced in the Trigger, Waveform, and Listing menus. You can display from 1 to 16 characters of the symbol name.

Symbol name field

When you first access the symbol table, there are no symbols specified. The symbol name field reads "New symbol." Select this field to enter a symbol name. When you are done, a symbol Type field becomes active.

Type field

The symbol Type field toggles between pattern and range. When the symbol is defined as a pattern, a Pattern/Start field appears to the right of the Type field. To assign a pattern, select the Pattern/Start field and type in the desired pattern.

If the symbol is defined as a range, a Pattern/Start field and a Stop field appear. Use these fields to specify the upper and lower boundaries of the range. To assign values to the boundaries, select the fields and enter the pattern. You can specify ranges that overlap or are nested within each other.

Label fields

The label fields are the fields with label names along the left side of the display below the field captioned Labels. The default label names are Lab1 through Lab126. Selecting the label fields pops up a choice of Turn Label On, Turn Label Off, and Modify Label.

The Turn Label Off option turns off the label. When a label is turned off, the label name and the bit assignments are saved by the logic analyzer so that you can turn the label back on and not have to retype the bit assignments and name. With labels off, the label names remain displayed for identification and searching purposes. Turning labels off may save memory in transitional timing.

Labels may have from 1 to 32 channels assigned to them. If you try to assign more than 32 channels to a label, the logic analyzer will beep, indicating an error. A message will appear at the top of the screen telling you that 32 channels per label is the maximum.

Channels assigned to a label are numbered from right to left by the logic analyzer. The least significant assigned channel on the far right is numbered 0, the next assigned channel is numbered 1, and all other channels are assigned sequentially up to the maximum of 16 per pod. Because 32 channels can be assigned to one label at most, the highest number that can be given to a channel is 31.

Although labels can contain split fields, assigned channels are always numbered consecutively within a label.

Label polarity fields

The label polarity fields, which are located just after the label, are used to assign a polarity to each label. The default polarity for all labels is positive (+). You change the label polarity by toggling the polarity field.

When the polarity is positive, 1 is high and 0 is low. When the polarity is negative, 1 is low and 0 is high. All data as well as bit-pattern specific configurations used for identifying, triggering, or storing data reflect the change of polarity. Numbers use the appropriate logical encoding, but waveforms and edges are still shown as logic levels – either low or high. In a timing analyzer with the data inverted, the waveform display remains positive true.

As an example, setting the logic analyzer to trigger on 0A hex with positive polarity is the same as setting it to trigger on F5 hex with negative polarity. The listing would show 0A with + polarity, F5 with - polarity. In the waveform menu, if the waveform is defined as bus the waveform shown as symbols inverts with a change of polarity. If the waveform is defined as individual channels or is not using symbols, it is not affected by changing polarity.

Trigger sequence levels

Sequence levels are the definable stages of the total trigger specification. Individual sequence levels are assigned using either a predefined trigger macro or a user-level trigger macro. The total trigger specification can contain both kinds of macro.

See Also Chapter 4, "Using the Trigger Menu," for more on setting up a trigger.

Sequence level usage

Generally, you would think using one macro in one sequence level uses up one of the available sequence levels. This may not always be the case. Some of the more complex predefined macros require multiple sequence levels. Keep this point in mind if you are near the limit on remaining sequence levels. The exact number of internal levels required per macro, and the remaining available levels, are shown within the macro library list. User macros, however, use only one level almost all the time. The only instance where multiple levels are used with the User macro is when the "<" duration is assigned.

Modify Trigger field

The Modify Trigger field allows you to modify the statements of any single sequence level as well as perform other high-level actions like global clearing of existing trigger statements, and adding or deleting sequence levels. Break Down Macros/Restore Macros acts a bit differently than the others.

Break Down Macros / Restore Macros

When a predefined macro is broken down, the contents of that macro are displayed in the same long form used in the User macro. If the macro uses multiple internal levels, all levels are separated out and displayed in the sequence levels of the Trigger menu. Once the macros in your trigger specification are broken down, Break Down Macros changes to Restore Macros. Use Restore Macros to restore all macros to their original structure.

When the macro is in a broken-down form, you can change the structure. However, when the macros are restored, all changes are lost and any branching that is part of the original structure is restored.

Use Break Down Macros if you want to view a particular macro part in its long form to see the exact sequence flow. Breaking down macros can also help in creating a custom trigger specification.

When a macro is broken down, you have all the assignment fields and branching options available as though they were a set of User macros. For information on the assignment fields, branching, occurrence counters, and time duration function, refer to Chapter 4 on the mechanics of creating a trigger level.

Timing trigger macro library

The following list contains all the macros in the library of timing trigger macros. They are listed in the same order as they appear onscreen.

User Mode

User level - custom combinations, loops

The User level is a user-definable level. This level offers low-level configuration and uses one internal sequence level. If the "<" duration is used, four levels are required.

Basic Macros

1. Find anystate "n" times

This macro becomes true when the first state it sees occurs "n" number of times. It uses one internal sequence level.

2. Find pattern present/absent for > duration

This macro becomes true when it finds a designated pattern that has been present or absent for greater than or equal to the set duration. It uses one internal sequence level.

3. Find pattern present/absent for < duration

This macro becomes true when it finds a designated pattern that has been present or absent for less than the set duration. It uses four or five internal sequence levels.

4. Find edge

This macro becomes true when the designated edge is seen. It uses one internal sequence level.

5. Find Nth occurrence of an edge

This macro becomes true when it finds the designated occurrence of a designated edge. It uses one internal sequence level.

Pattern/Edge Combinations

1. Find edge within a valid pattern

This macro becomes true when a selected edge type is seen at the same time as a designated pattern. It uses one internal sequence level.

2. Find pattern occurring too soon after edge

This macro becomes true when a designated pattern is seen occurring within a set duration after a selected edge type is seen. It uses three or four internal sequence levels.

3. Find pattern occurring too late after edge

This macro becomes true when one selected edge type occurs, and for a designated period of time after that first edge is seen, a pattern is not seen. It uses two internal sequence levels.

Time Violations

1. Find 2 edges too close together

This macro becomes true when a second selected edge is seen occurring within a designated period of time after the occurrence of a first selected edge. It uses three or four internal sequence levels.

2. Find 2 edges too far apart

This macro becomes true when a second selected edge occurs beyond a designated period of time after the first selected edge. It uses two internal sequence levels.

3. Find width violation on a pattern/pulse

This macro becomes true when the width of a pattern violates designated minimum and maximum width settings. It uses four or five internal sequence levels.

Delay

- Wait "t" seconds

This macro becomes true after a designated time period has expired. It uses one internal sequence level.

State trigger macro library

The following list contains all the macros in the library of state trigger macros. They are listed in the same order as they appear onscreen.

User Mode

User level - custom combinations, loops

The User level is a user-definable level. This level offers low-level configuration and uses one internal sequence level.

Basic Macros

1. Find anystate "n" times

This macro becomes true when the first state it sees occurs "n" number of times. It uses one internal sequence level.

2. Find event "n" times

This macro becomes true when it sees a designated pattern occurring a designated number of times consecutively or nonconsecutively. It uses one internal sequence level.

3. Find event "n" consecutive times

This macro becomes true when it sees a designated pattern occurring a designated number of consecutive times. It uses one internal sequence level.

4. Find event 2 immediately after event 1

This macro becomes true when the first designated pattern is seen immediately followed by a second designated pattern. It uses two internal sequence levels.

Sequence Dependent macros

1. Find event 2 "n" times after event 1 before event 3 occurs

This macro becomes true when it first finds a designated pattern 1, followed by a selected number of occurrences of a designated pattern 2. In addition, if a designated pattern 3 is seen anytime while the sequence is not yet true, the sequence starts over. If pattern 2's "nth" occurrence is coincident with pattern 3, the sequence starts over. It uses two internal sequence levels.

2. Find too few states between event 1 and event 2

This macro becomes true when a designated pattern 1 is seen, followed by a designated pattern 2, and with less than a selected number of states occurring between the two patterns. It uses three or four internal sequence levels.

3. Find too many states between event 1 and event 2

This macro becomes true when a designated pattern 1 is seen, followed by at least a selected number of states, then followed by a designated pattern 2. It uses two internal sequence levels.

4. Find n-bit serial pattern

This macro finds an "n" bit serial pattern on a designated channel and a designated label. It uses "n" internal sequence levels.

Time Violations

1. Find event 2 occurring too soon after event 1

This macro becomes true when a designated pattern 1 is seen, followed by a designated pattern 2, and with less than a selected time period occurring between the two patterns. It uses two internal sequence levels.

2. Find event 2 occurring too late after event 1

This macro becomes true when a designated pattern 1 is seen, followed by at least a selected time period, before a designated pattern 2 occurs. It uses two internal sequence levels.

Delay

1. Wait "n" external clock states

This macro becomes true after a designated number of user clock states have occurred. It uses one internal sequence level.

Modifying the user macro

Before you begin building a trigger specification using the user macro, it should be noted that in most cases one of the predefined trigger macros will work.

If you need to accommodate a specific trigger condition, or you prefer to construct a trigger specification from scratch, use the User macro as a starting point. This macro appears in long form, which means it has the analyzer's total flexibility available in terms of resource terms, global timers, occurrence counters, duration counters, and two-way branching.

The User macro has a "fill-in-the-blanks" type statement. You have the following elements to use:

- Bit Patterns, Ranges, and Edges
- Storage Qualification
- < and > Durations
- Occurrence Counters
- Timers
- Branching

A typical method used during a debug operation is to first trigger on a known pattern, edge or range. From that point, it becomes an iterative process of adding more levels to further filter the data. It is important for you to know how to use such elements as occurrence counters, timers, and branching, to zero in and trigger at the desired point.

As the analyzer executes the trigger specification, it searches for a match between the resource term value and the data. When a match is found, that part of the sequence statement becomes true and the sequencing continues to the next part of the statement or the next sequence level.

Eventually a path of "true" resource terms leads to your trigger command. If timers or occurrence counters are used, the analyzer waits or counts occurrences of a specified value before continuing.

The following examples illustrate the use of resource terms, occurrence counters, timers, branching, and store qualification. You will use them in your trigger specification either by themselves or combined with each other.

Using bit patterns, ranges, and edges

Bit patterns are set to match specific data values, and ranges are set to match a range of bit patterns. In the Timing Acquisition mode, edges are set to match specific edges of a timing pulse.

Using storage qualification

Store qualification lets you store all data, no data, or just selected data, before trigger occurs.

Setting < and > durations (Timing only)

When a resource term is found during a timing sequence evaluation, you can dictate how long the term must remain before it actually becomes true. When less than (<) or greater than (>) duration is assigned, the secondary branching (Else on) is not available.

> field When greater than (>) is used, the analyzer continues sequence level evaluation only after the resource term has been true for greater than or equal to the amount of duration specified.

< field When less than (<) is used, the analyzer continues sequence level evaluation only after the resource term has been true for less than or equal to the amount of duration specified. Using less than requires four sequence levels.

Using the Occurrence Counters

Occurs field When "Occurs" is selected, the < and > duration functions change to an occurrence counter. Use the occurrence counter to delay sequence evaluation until the resource term has occurred a designated number of times. If the "else on" branch becomes true before all specified occurrences of the primary "Trigger on" branch, the secondary "else on" branch is taken.

Using the timer

Timers are like other resource terms in that they are either true or false. Timers can be set to Start, Stop, Pause, or Continue as the analyzer enters a sequence level. The two timers are global, so each sequence level can control the same timer. The default timer condition in all sequence levels is Off.

Timers start as you enter the sequence level, and when the timer count expires, the timer becomes true. If a timer is paused in one level, it must be continued in another level before it can count through.

As more sequence levels are added, the timer status in the new levels defaults to Off. Timers must be continued or started in each new level as appropriate. When a timer expires or stops, its count resets to zero.

Branching

If either the less than or greater than duration is used, only the primary branch is available. Otherwise, each sequence level except for the last has two-way branching.

If the primary branch is taken, the analyzer goes to the next level. If the primary branch is not found, the analyzer immediately evaluates the "Else on" secondary branching term.

If the "Else on" term is found, the secondary branch taken is to the designated sequence level. If the "Else on" term is not found, the analyzer continues to loop within the same sequence level until one of the two branches is found. If the "Else on" branch is taken, the occurrence counter is reset even if the "go to level" branch is back to the same level. If both branches are found true at the same time, the primary branch is taken.

Branching across the trigger level is possible. If this occurs, the sequence level evaluation could loop without ever seeing a trigger term. Be careful in designing your sequence instructions.

Resource terms

Resource terms are user-defined variables that are assigned to sequence levels. They are placed into the sequence statement where their bit pattern or edge type is searched for within the data stream. When a match is found, a branch is initiated and the next statement or sequence level is acted upon. Resource terms take the following forms:

- Bit pattern terms a–j
- Range terms 1 and 2
- Edge terms 1 and 2 (Timing only)
- Global timers 1 and 2

All resource terms and timer terms are listed in a scrollable Terms field. To view all offscreen terms, select the Terms field, then use the knob to roll the terms list onscreen.

When the logic analyzer is configured as a state analyzer, you can use any of the ten bit pattern terms, range terms, or timers in your trigger specification. When you configure the logic analyzer as a timing analyzer, you can use any of these terms plus the edge terms.

Bit pattern terms a–j

You can set a bit pattern consisting of any combination of 1s, 0s, or Xs (don't cares) for the 10 terms a – j. Bit pattern terms can also take the NOT form of a – j.

Range terms 1 and 2

Two range terms are available which can be set to a range of bit pattern values. The first pattern and the last pattern are part of the range which must be matched.

Range terms take the form of either In Range, or the NOT form of Out Range.

Edge terms 1 and 2 (Timing only)

The two edge terms are only available in the timing analyzer. Each edge term is assigned positive-going, negative-going, or any-transition edge type.

Global timers 1 and 2

In addition to the resource terms available, there are two global timers available. Each timer can be started, paused, continued, or stopped from any sequence level except the first.

Assigning resource term names and values

The Terms field identifies the list of available resource terms within the analyzer. A resource term can be assigned to only one machine at a time. The resource term names (a – j, Edge1, Edge2, Range1, Range2) are default names that can be changed. You assign values in the following two ways:

- Using Preset Values
- Assigning Bit by Bit

Changing resource properties When any of the individual term fields are selected, a configuration pop-up menu appears. Use this pop-up menu to quickly set the resource term to a preset value.

Using Preset Values

Assign Assign toggles which machine the term is assigned to. All of the available resource terms except the Edge terms can be assigned to any analyzer. However, a term can only be assigned to one analyzer at a time.

Rename Rename lets you change the term name. This function works for all terms.

Clear (=X) Clear sets the terms to their broadest possible meaning. For terms a – j, the assignment field is set to all Xs (don't cares). For Range 1 and 2, the boundaries are set to the maximum and minimum values. For Timers 1 and 2, the assignment field is set to a minimum time of 400 ns. For Edge 1 and 2, the assignment field is set to don't cares.

Set (=1) In terms a – j, the assignment field is set to its maximum value, with all bits set to 1. This option is not available for the Range, Timer, and Edge terms.

Reset (=0) In terms a – j, the assignment field is set to its minimum value, with all bits set to 0. This option is not available for the Range, Timer, and Edge terms.

Assigning Bit by Bit

Bit pattern terms Just to the right of the bit pattern name fields are the term assignment fields. When any of the individual assignment fields are selected, a keypad appears. Use this keypad to assign real values or Don't Care (X) values.

Edge terms Assign edge terms the same way you do bit pattern terms. Edge terms can be used singularly or in combination with each other across all assigned channels. When you specify an edge on more than one channel, the analyzer ORs the edges.

After the assignment menu closes, you may see "$" indicators in the field display. A "$" indicates the assignment can't be displayed in the selected base because of Don't Cares. When you display the assignment in binary, however, you can see the actual pattern.

Range terms Range terms require an upper and lower bit pattern boundary. The range is recognized as the data that is numerically between or on the two specified boundaries. In addition, the range must be contained in a single label across a single pod pair, with no clock bits allowed.

Timer terms Timers are either true or false. Timers start as you enter the sequence level, and when the count expires, the it becomes true. If a timer is paused in one level, it must be continued in another level before it can count through.

As more sequence levels are added, the timer status in the new levels defaults to Off. Timers must be continued or started in each new level if it is appropriate. When a timer expires or stops, its count resets to zero.

Combination of terms

Combination terms are configured and selected from within trigger sequence levels. All user-defined resource terms can be combined to create complex qualifiers that occupy a single assignment field space.

When you select the term field in a Sequence Level menu, a pop-up selection list appears. If you then select "Combination," a logical assignment menu appears. Use this menu to turn on resource terms and input them into a chain of logical operators.

When the combination is placed in the assignment field, if the term is too long to fit in the assignment field, the display is truncated.

Arming Control field

Arming Control sets up the order of triggering for complicated measurements involving more than one machine. You can set the logic analyzer to begin running when it receives a signal from an external machine, have one analyzer start the other, or have one analyzer send a signal to another external machine. The default configuration has both analyzers running independently without external communications.

Arming control between analyzers

If both analyzers are turned on, you can configure one analyzer to arm the other. When you select the analyzer name in the Arming Control menu, a pop-up menu for selecting where the Arm In signal is coming from appears. This pop-up menu also selects the sequence level in which an "arm" flag is placed.

When an analyzer receives an Arm In signal, the arm term in the user-selected sequence level becomes true. If the analyzer was waiting at a trigger sequence level for the arm term, the analyzer begins evaluating the rest of that sequence level. However, if the arm term is not part of the current sequence level, the preceding sequencing could trigger the analyzer before the arm term is seen. Generally, the arm term is evaluated and used the same as the other resource terms within the sequence instruction.

Arming control using external BNCs

A more complex arming example involves passing arm signals in and out through the External BNCs on the rear panel. In the Arming Control menu, the External Triggers are called "Port In" and "Port Out". The leftmost field toggles between "Run" and "PORT IN", and the rightmost toggles between "Off" and "PORT OUT".

One possible scenario is to have several test instruments and a logic analyzer connected to a complex target system. The analyzer is armed by an external Arm In signal from another test/measurement entity. After the first analyzer triggers, it arms the second analyzer. After the second analyzer triggers, it sends a Port Out signal through the external BNC. This signal is used to arm another external test/measurement entity.

The Arm Out signal can be generated by either one of the two local analyzers.

Acquisition Control field

Selecting the Acquisition Control field pops up the Acquisition Control menu. The Acquisition Control menu sets the acquisition mode, the trigger position within acquisition memory, and the sample period.

Acquisition Mode field

The Acquisition Mode field toggles between Manual and Automatic. When set to Automatic, the position of stored data relative to trigger and the sample rate are based on the sec/Div and delay settings in the Waveform menu.

When Acquisition Mode is set to Manual, additional configuration fields become available. The additional configuration fields work together with the sequence instructions in a prioritized manner to position the memory relative to the trigger point. A small picture at the bottom of the menu displays the sum effect of all the settings on the trigger position within memory.

Trigger Position field

The Trigger Position field sets how much information is stored before and after the trigger. When a run is started, a timing analyzer will not look for a trigger until at least the proper percent of pre-trigger data has been stored. A state analyzer will trigger at the first occurrence of the trigger, but will notify you that the prestore was not completed. After a trigger has been detected, the rest of memory is filled before the analyzer halts.

In a timing analyzer, even when the trigger position is set to Start or End, there will always be a small portion of pre-trigger and post-trigger data stored. Most of the choices designate prestore and poststore percentages, but the Delay setting affects when the memory begins storing data relative to the trigger.

Delay The Delay field delays the start of acquisition storage after the trigger. The delay time range is affected by the sample period but could range from 16 ns to 8 ks. As the picture in the pop-up menu shows, any data falling between the trigger and the delay time is not stored.

Branches Taken Stored / Not Stored field

The Branches Taken field is a toggle field that sets the analyzer to store, or not to store, the resource term that sent the analyzer off on a branch.

As the analyzer steps through the sequence instructions, it may take either branch of a sequence level. With Branches Taken set to Stored, the state

data values that caused the branch are stored. When the analyzer is set to Branches Taken Not Stored, only the data you explicitly designate in the sequence levels is stored.

The Branches Taken Stored/Not Stored is not available when the analyzer is configured as a timing analyzer.

Count field (State only)

The Count field accesses a selection menu which indicates whether acquisition data is stamped with a Time tag or a State Count tag.

Time and State tags

If you have all pod pairs assigned, the state acquisition memory is reduced by half when time or state tags are turned on. You can maintain full memory depth if you leave a specified pod pair unassigned.

States States places numbered tags on all data relative to the trigger. Pre-trigger data has negative numbers and post-trigger data has positive. In the display menus, State numbering is either relative to the previous memory location or absolute from the trigger point. You can set it in the display menus by toggling the Absolute/Relative field.

Time Count time places time tags on all displayed data. Data stored before triggering has negative time numbers and data stored after triggering has positive time numbers. Time tag numbering is set to be either relative to the previous memory location or absolute from the trigger point. Selecting the Absolute or Relative option is done by toggling the Absolute/Relative field. Time tag resolution is 8 ns.

To retain full memory using time or state tags To retain full memory depth when using time or state tags requires that one pod pair be unassigned. The exact pair to unassign varies. Generally, it is best to unassign one of the middle pod pairs. If you have two analyzers configured, the ends must be assigned to different analyzers.

Markers

The Markers field accesses the markers selection menu. When the Markers field is selected, a marker selection menu appears with the marker choices appropriate for the present analyzer configuration.

Off

The Off selection turns off marker operations but does not turn off operations based on the markers. For example, if a stop measurement was previously specified and the stop measurement criteria are met, the measurement will stop even though the markers are off.

Pattern markers

Pattern markers identify and mark unique bit patterns in the data listing. Once the unique bit patterns are marked, you can use them as reference points or as criteria for a stop measurement.

When a marker is positioned in the Listing menu, it is also positioned in the Chart menu and Waveform menu, but not in the Mixed Display menu.

State analyzer markers

In a state analyzer with Count Off in the Trigger menu, only Pattern markers are available. With Count Time turned on, Time markers and Statistics markers become available. With Count States turned on, State markers become available.

Timing analyzer markers

Timing analyzers always have marker choices of Pattern, Time, or Statistics. Timing analyzers do not have state markers. The pattern markers, though, can be used to count intervening patterns.

Stop measurement field

The stop measurement function specifies a condition that stops the analyzer measurement during a repetitive run. If two analyzers are configured, both analyzers stop when either specified stop condition is satisfied.

Off The Off selection turns all Stop measurement operations off. If the stop measurement operation is not turned off and the stop measurement criteria is met, the measurement will stop even though the markers are set to other types or turned off.

X-O The X-O option is available in the Timing analyzer and in the State analyzer with its count set to Time.

When X-O is selected, a repetitive run is stopped when a comparison of the time period between the X and O markers and one of the time period options is true.

Compare When you select Compare, a repetitive run is stopped when a comparison of data in the Listing menu and data and criteria in the Reference listing of the Compare menu matches an equality selection. The equality selection is set from the Equal/Not Equal selection pop-up menu.

Statistics markers

After patterns are assigned to the X and O markers, statistical information is available when markers are set to Statistics.

In a State analyzer, Statistics markers only become available when the Trigger menu Count field is set to Time.

Statistics are based on the time between the X and O. Both markers must be found before valid statistical information is displayed.

sec/Div field

When acquisition control is set to automatic, the sec/Div field affects the sample period. Timing waveforms are reconstructed relative to the sample period. A shorter sample period puts more sample points on the waveform for a more accurate reconstruction but also fills memory more quickly.

If the sec/Div is changed resulting in a change in the next sample period, you must run the analyzer again before the current sample period display is updated. The sample period is shown in the second row from the top when the markers are turned off.

Accumulate field

The Accumulate field controls whether old data is cleared or displayed along with new data. The Accumulate field will toggle On/Off. When Accumulate is on, the analyzer displays the data from a current acquisition on top of the previously acquired data. When Accumulate is off, the display is cleared before each new run cycle.

If you leave the Waveform menu, or pop up a menu over the waveform display, any accumulated display data is lost and the accumulation process starts over.

Delay field

Depending on the analyzer configuration, a positive or negative delay measured in either states (State only) or time (Timing only) can be set. The Delay field lets you scroll the data and place the display window at center screen. Changing the delay will not affect the data acquisition unless it is a timing analyzer and the acquisition mode is automatic. In this case, the sample period changes.

The delay range of a timing analyzer is from –2500 seconds to +2500 seconds. The delay range of a state analyzer is from –8192 states to +8192 states.

Waveform label field

The waveform label field, located on the left side of the waveform display, is both a display and configuration field. After all desired waveforms are configured for display, they are listed in the waveform label field. If there are more waveforms than can be displayed, you can roll the list by selecting the waveform label field, then after the roll indicator appears, turn the knob.

If the waveform label field is selected a second time, a waveform modification menu appears. Use this menu to configure the waveform display.

When the waveform modification menu appears, select the operation to insert, replace, delete, or scale waveforms into the display. You can display a maximum of 24 waveforms on screen at one time.

Viewing state values in the bus option

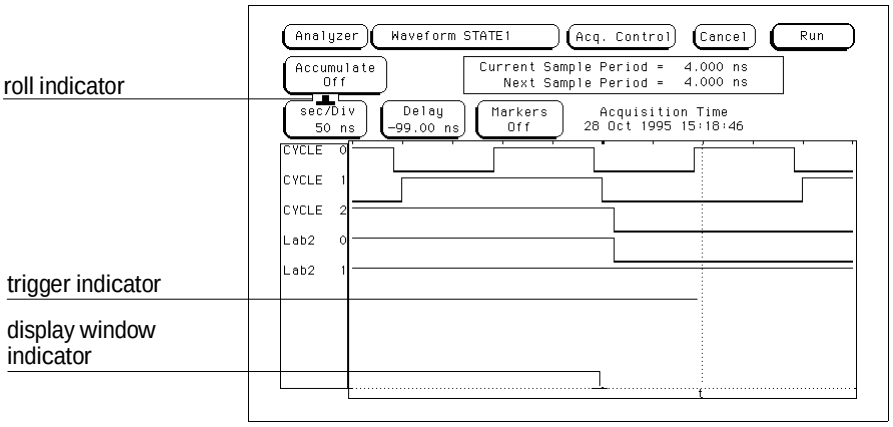
When all assigned waveforms in a label are overlaid with the Bus option, the value of the data is displayed in the base selected in the Listing menu to the right of each new transition in the waveform display. This happens only when the waveform size is set to large.

If the sec/Div is set to view a large increment of time, or the waveform scaling is set to small or medium, the state data readout does not fit between transitions. To display the state data readouts within the waveform, expand the sec/Div and use the large waveform setting.

Waveform display

At the bottom of the Waveform menu is a reference line which displays the relative location of the display window, the markers, and the trigger point with reference to the total memory.

Total memory is represented by a horizontal dotted line. The display window is represented by an overlaid solid line. The markers and trigger point are represented by small dots above the total memory line, and an X, O, and t label, all of which are located below the total memory line.



Waveform Display

The Mixed Display Menu

The Mixed Display menu combines a state listing display located at the top of the menu and a waveform display located at the bottom of the menu. The Mixed Display menu shows both state and timing data in the same display.

The Mixed Display menu only becomes available when at least one analyzer is configured as a state analyzer, with its Count field in the Trigger menu set to Time. If two state analyzers are configured, both state listing displays can be interleaved as well as shown separately, however, the listing menus are the best display menus for a two-state analyzer configuration.

The waveform display area shows timing analyzer waveforms from the configured timing analyzer.

Interleaving state listings

Interleaved state listings lets you view two labels and their data from different analyzers in the same column. The process of interleaving state listings can be performed in either the Listing menu or the Mixed Display menu. For example, if data is interleaved in the Listing menu, it will be automatically interleaved in the Mixed Display menu.

The interleaved label is placed directly above the selected label, and all interleaved data is displayed in white. In addition, the state numbers of the interleaved data are indented to the right. Because of the lack of room available in the listing portion of the Mixed Display menu, the label identifying the interleaved data is not displayed. For this reason, when two state analyzers are configured the listing menus should be used to display interleaved labels.

Time-correlated displays

Once the Time markers are set in the Waveform display area of the Mixed Display menu, time-correlated X and O Time markers will be displayed in both the listing and the waveform display areas.

Markers

The markers in the Mixed Display menu are not the same as the markers in the individual Listing and Waveform menus. First, Mixed Display only has time markers. Second, markers placed in the individual waveform and listing menus will not transfer to the Mixed Display menu. You must place new Time markers on your points of interest in the Mixed Display.

State Chart is a software post-processing feature that provides the ability to build x-y charts of label activity using state data. The Chart menu builds a graphical representation of the system under test. The Y axis always represents data values for a specified label. You can select whether the X axis represents states (rows in the state listing) or the data values for another label.

When the X-axis is set to State, X and O markers are available which display the current sample relative to the trace point and the corresponding Y-axis data value. Marker placement is synchronized with the normal state listing.

An accumulate mode is available that allows the chart display to build up over several runs.

You can generate x-y charts of Label vs. Label or Label vs. State.

Label vs. Label charts

When labels are assigned to both axes, the chart shows how the data acquired under one label varies relative to the other for a particular measurement. Label values are always plotted in ascending order from the bottom to the top of the chart and in ascending order from left to right across the chart. Plotting a label against itself will result in a diagonal line from the lower left to upper right corner. All markers are disabled when plotting this kind of chart.

Label vs. State charts

Label versus State is a plot of data values acquired under a label versus the memory location of the same data. The label value is plotted against successive memory location numbers.

Min and Max scaling fields

When State is selected for the X axis, the minimum and maximum values can range from –8192 to +8192 depending on the trace point location.

When Label is selected for either axis, the minimum and maximum values range from 00000000 hex to FFFFFFFF hex regardless of the axis, because labels are restricted to 32 bits.

Markers/Range field

The Marker/Range field is a toggle field. If the field is set to Range, X and Y range fields become available to set the chart minimum and maximum range points. If the field is set to Markers, a marker selection menu appears with marker choices available with the present analyzer configuration.

In a state analyzer with Count Off in the Trigger menu, only Pattern markers are available. With Count Time on, Time markers and Statistics markers become available. With Count States on, States markers are available. The markers function just like those of the Waveform and Listing displays.

State Compare is a software postprocessing feature that compares bit-by-bit the acquired state data listing and a reference listing. State Compare is only available when at least one analyzer is configured as a State analyzer.

The comparison between the acquired state listing data and the data in the reference listing is done relative to the trigger points. This means that the two data records are aligned at the trigger points and then compared bit-by-bit.

Any bits in the acquired data that do not match the bits in the compare image are treated as unequal.

You can separately view the acquired data, the reference listing, and a listing that highlights the bits in the acquired data that do not match the corresponding bits in the reference listing.

You can edit the reference listing for unique comparisons.

You can mask specific bits that you do not want to compare. These "Don't compare" bits can be specified individually for a given label and state row, or specified by channel across all state rows.

You can select a range of states to compare. When a range is selected, only the bits in states on or between the specified boundaries are compared. Also, you can save the reference listing along with the analyzer configuration to disk.

Reference Listing field

The Reference Listing field is a toggle field that switches the listing type between the Reference image listing and the Difference listing.

The Reference listing is a display of the image (or template) that acquired data is compared to during a comparison measurement. The boundaries of the image (or size of the template) are controlled by using the channel masking and compare range functions. Any bits in the reference listing displayed as "X" have been set to don't care bits during bit editing.

When the data listing is rolled, the difference data listing and the data listing in the Listing menu are also rolled.

Difference Listing field

The Difference Listing field is a toggle field that switches the listing type between the Reference image listing and the Difference listing.

The Difference listing is a display of the acquired data listing with the data that differs, if any, from the Reference listing, highlighted with inverse video. If the base is inverse assembled symbols, the entire line is highlighted with inverse video.

The controls that roll the listing in all three menus (the normal State listing, the Reference listing, and the Difference listing) are synchronized unless the number of pre-trigger states differ between the Reference listing and the acquired data.

This means that when you change the current row position in the Difference listing, the analyzer automatically updates the current row in the acquired State listing and Reference listing, and vice-versa.

If the three listings are synchronized and you acquire data again, the Reference listing may have a different number of pre-trigger states depending on the trigger criteria. The Reference listing can be resynchronized to the State and Difference listings by entering the desired state (acquisition memory) location from the front-panel keypad.

This lets you view corresponding areas of all lists, to cross check alignment, and to analyze the bits that do not match.

Copy Listing to Reference field

The initial Reference image is generated by either copying the data listing from the listing menu or by loading an analyzer configuration file which contains a Reference listing. Be aware that if you load an analyzer configuration to get a Reference image, the other menu setups will change.

When the Copy Listing to Reference field is selected, the contents of the acquisition data structure (Listing menu display)are copied to the Reference image buffer. The previous Reference image is lost if it has not been saved to a disk.

Find Error field

The Find Error field lets you easily locate any patterns that do not match in the current comparison. Occurrences of differences or errors are found in numerical ascending order from the start of the listing. The first occurrence of an error has the numerical value of one.

You select which error number to find by highlighting the Find Error field and entering a number from the front-panel keypad. If the roll indicator is in the Find Error field, simply turn the knob. The listing is then scanned sequentially until the specified occurrence is found and rolled into view.

Compare Full/Compare Partial field

The Compare Full/Compare Partial field is a toggle field which lets you compare either the full range of states or define a subset of the total number of states in the Reference image to be used in the comparison.

The Compare mode is accessed by selecting the Compare Full/Compare Partial field in either the Compare or Difference listing menus. When selected, a pop-up appears in which you select either the Full or Partial option.

When you select the Partial option, fields appear for setting the start state and stop state values. Only bits in states (lines) on or between the boundaries are compared against the acquired data.

Mask field

The channel masking field is used to specify a bit, or bits in each label that you do not want compared. This causes the corresponding bits in all states to be ignored in the comparison. The Reference data image itself remains unchanged on the display.

When you select the Mask field an assignment pop-up appears in which you specify which channels are to be compared and which channels are to be masked. A "." (period) indicates a don't compare mask for that channel and an "*" (asterisk) indicates that channel is to be compared.

Bit Editing field

The bit editing fields are located in the center of the Reference listing display. A bit editing field exists for every label in the display unless the label's base is ASCII or inverse assembled symbols. The bit editing field lets you modify the values of individual bits in the Reference image or specify them as don't compare bits.

You access data in the Reference listing by rolling the data listing using the knob until the data is located in the bit editing field. To enter a desired pattern or don't compare (X) for a bit, select the field and use the front-panel keypad.

System Performance Analysis (SPA) Software

System Performance Analysis Software

The System Performance Analysis (SPA) software is included as standard software in the HP 1660C/CS/CP-series logic analyzers. It was originally HP 10390A System Performance Analysis (SPA) Software, a software package for the HP 16550A logic analyzer module and the HP 1660A/AS-series logic analyzers.

SPA provides you with a set of functions for performing statistical analysis on your target system. Its functions include State Overview, State Histogram, and Time Interval modes.

To be successful with this software, you should be familiar with the operation of the logic analyzer.

The screen shots shown in this chapter are HP 16550A screens. This chapter is organized as follows:

- "What is System Performance Analysis?" outlines typical SPA applications, and describes the operating characteristics for each SPA mode.
- "Getting started" describes how to access the SPA menus and how to select the SPA modes and set the specifications.
- "SPA measurement processes" is a detailed description of the measurement processes used by the SPA package. This theory of operation explains how the SPA software samples and sorts the data from the target system, and how the onscreen measurement values are computed for the State Overview, State Histogram, and Time Interval modes.
- "Using State Overview, State Histogram, and Time Interval" leads you through the State Overview, State Histogram, and Time Interval modes. It also tells how to set up SPA for the three modes, how to interpret the acquired data, and how to make measurements on specific areas of interest.
- "Using SPA with other features" tells you how to use SPA with other features.

Error messages and warnings used by SPA are the same as those used by each of the logic analyzers. Refer to "Troubleshooting," Chapter 11, for descriptions of these messages.

If you need programming information, refer to the *HP 1660C/CS/CP-Series Logic Analyzers Programmer's Guide*, available from your HP Sales Office.

What is System Performance Analysis?

The logic analyzer's state or timing analyzer is used to make quantitative measurements on specific events in the target system. For example, they can measure a specific time interval on a microprocessor's control lines or can find out how a particular subroutine was called.

System Performance Analysis, on the other hand, is used for qualitative measurements on the target system. SPA provides statistical analysis functions so you can determine how efficiently your target system is operating.

SPA repeatedly samples signals of interest, such as an address bus or the output of a counter. The multiple data sets from the repeated sampling are then used to build histograms and compile statistics that describe your target system's performance over time.

Some typical examples of SPA applications include:

- Obtain an overview of system activity.
- Identify software problems that lock up the microprocessor.
- Determine the best-case and worst-case execution times for a software module or a state machine.
- Establish standards for software modules or state machines.
- Identify inefficient use of mass storage and other peripherals.
- Evaluate memory utilization, such as illegal access in protected portions of memory, and locality of execution.

Operating characteristics

The following describes the operating characteristics of the System Performance Analysis software for the three SPA measurement modes.

State Overview The State Overview mode displays a bar chart of a label's state value versus the relative number of occurrences of each value in the defined range of the label. State Overview is available on any label defined in the Format Specification.

- The X axis is the defined range for the specified label which is divided into 256 buckets.
- The range of the specified label is user-definable.

- The Y axis is the relative number of occurrences in each bucket.
- The maximum value of the Y axis is constantly updated to reflect the number of occurrences in the bucket that has the most occurrences, and is displayed as "Max count".
- The total number of states sampled for the selected label is presented as Total count. This includes states that may be outside the user-specified X axis range.
- Two markers are available on the X axis to determine the range of a bucket and number of occurrences in any bucket.
- Choice of base for a specified label is user-definable.

State Histogram The State Histogram mode displays states that occur within user-defined ranges of a label. State Histogram is available on any label defined in the Format Specification.

- The maximum number of ranges is 11.
- Other States included/excluded is available and displays a histogram of all states not covered by the user-defined ranges.
- You can trace All States or patterned Qualified States.
- Total samples displays the total number of occurrences in all displayed ranges.
- The choice of base for specified label is user-definable.

Time Interval The Time Interval mode displays time intervals between user-defined start and end events.

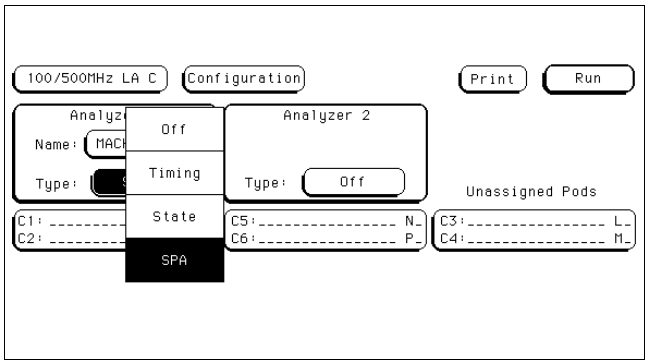
- Start and end events can be defined over all labels defined in the Format Specification.
- 10 ns is the minimum sample period and time interval resolution.
- The maximum number of time interval ranges is 8.
- The time interval range size is 10 ns to 9,999,999 seconds.
- Calculated statistics provides Maximum time, Minimum time, Average time, and Total number of time intervals sampled (one time interval defined to be a paired start/end event).
- The auto-range feature automatically scales the eight time intervals over maximum and minimum times using a logarithmic scale or linear scale.
- Choice of base for labels is user-definable.

Getting started

This section describes how to access the System Performance Analysis (SPA) menus. Also, it describes selecting the SPA modes and setting the specifications.

Accessing the menus

The SPA menus are accessed through the Analyzer Configuration menu. When the configuration menu is displayed, select the Type field and choose SPA from the pop-up.



Configuring an Analyzer for SPA

Selecting State Overview, State Histogram, or Time Interval modes

To access one of the three SPA modes, select the analyzer menu field after configuring one of the analyzers as SPA and select SPA.

Once in the SPA menu, you can move from State Overview, State Histogram, or Time Interval Modes by selecting the Trace Mode field as shown in the SPA menu on the next page. A pop-up menu appears, and you can select one of the three SPA modes in the pop-up.

> If you change modes while the logic analyzer is acquiring data, it will stop the acquisition.

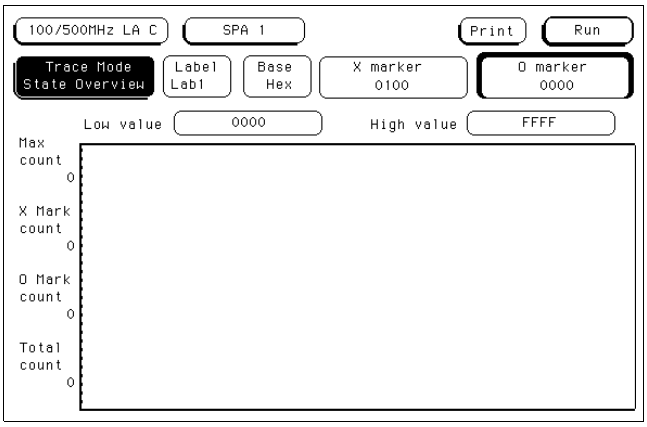
Setting up the State Format specification

When a State or Timing analyzer is changed to SPA, SPA will retain the State or Timing Format specification. For complete details on changing from a State or Timing Analyzer to SPA, see "Using SPA with other features."

The State and Timing format specification menus provide symbol tables. You can use any defined symbols to specify the Low and High values in State Overview to define the ranges and the qualified states in State Histogram, or to specify the Start and End conditions in Time Interval.

Your ability to use existing State or Timing configurations with SPA depends on your application and target system. If your SPA measurement uses the same physical signals from the target system as an existing State or Timing configuration, it may be easier to load the state or timing configuration from the disk instead of entering a new one.

This manual assumes you already have a basic understanding of the Analyzer Format menu, and it will not be covered here.



Default SPA Menu

SPA measurement processes

This section introduces you to the measurement processes of the System Performance Analysis (SPA) software. It tells you how to select the appropriate trace mode and labels. It also explains how SPA samples and sorts data.

Selecting and changing trace modes

SPA has three trace modes: State Overview, State Histogram, and Time Interval. These are selected by the Trace Mode field in the SPA data display.

Only the currently displayed trace mode is affected during an acquisition. While acquiring and viewing data in one trace mode, the other two trace modes are not updated. If the trace mode or any other critical variable is changed during an acquisition, the logic analyzer stops the acquisition and displays "Warning: Run HALTED due to variable change."

Each trace mode only performs statistics on its own database. Therefore, if acquisitions are completed in two different trace modes, the two modes will not contain the same data.

For example, you select the State Overview mode and press the Run key. After the data accumulates for a period, press Stop. You then select the Time Interval mode and the screen is blank since no data has been acquired in this mode. You again press Run, and let data accumulate and press Stop. In this example, two separate data sets are acquired, the first for State Overview mode, the second for Time Interval. You can now move between the modes and see the correct data for the associated measurement.

This separate acquisition data applies to all three trace modes. In this way, three separate views of the target system can be acquired and stored in SPA.

Sampling methods and data sorting

SPA provides a statistical summary of target system behavior over time. The greater the number of samples, the more accurate the statistics. Therefore, SPA should always be run in the Repetitive mode. By doing this, the analyzer will continue to sample the data and update the display until Stop is pressed or until a sampling variable is changed on the display.

After SPA completes an acquisition, each sample in the current acquisition is compared to the ranges or buckets for the current trace mode. If the sample matches a range or bucket, it is sorted into that range or bucket. This process is repeated for every sample in the acquisition. After the entire acquisition

has been sorted, the histograms and displayed statistics are updated, and the analyzer is re-armed for the next acquisition.

Refer to the following sections on the three trace modes for details on sorting criteria and statistical computation.

Between each successive acquisition, there is blind time during which the captured data is unloaded and sorted, the display is updated, and the analyzer is restarted. The length of the blind time is a function of the complexity of the SPA measurement.

Selecting and changing labels

A label in Hewlett-Packard logic analyzers is defined in the Format menu. A label is any named group of 32 or fewer data channels.

The State Overview and State Histogram modes monitor one label at a time. Any labels that are defined in the Format Specification are available. A typical example is the ADDR (address) label used in many of the Hewlett-Packard inverse assembler configurations. Often, SPA measurements will use the ADDR label to monitor memory activity.

Qualified State Histogram and Time Interval modes use all of the labels in the Format Specification to define either the qualified state or the start and stop events, respectively. While State Overview and State Histogram deal with recorded states, Time Interval deals with time.

Changing from one label to another in State Overview or State Histogram mode or changing the Start or End pattern in Time Interval erases any configuration and data for the original label. When returning to the original label, the display returns to its default mode. Loss of configurations and data when changing between labels can be prevented by saving configurations of interest to the disk before making the change, or by printing the results.

State Overview mode

State Overview mode is an X-versus-Y chart of the activity on a specified label. It provides a global view of the distribution of activity of the target system signals grouped under the specified label.

X axis scaling The X axis represents the defined range of the specified label and is divided into a series of buckets, or smaller ranges. The range of the X axis is defined by the Low value and High value fields, and is

divided equally among 256 buckets. For example, if the range defined by the low and high values is 1100, then 1100 divided by 256 equals 4.29. This value will be rounded up to 5, each bucket will have a range of 5, and only 220 buckets will be used (1100/5 = 220). The display grid will be truncated on the right because only 220 buckets are displayed.

If the full range of the label or the portion of the label defined by the Low value and High value is less than 255, then the number of buckets will be the difference between the Low and High values.

The Low and High values can be specified as discrete values in Binary, Octal, Decimal, or Hexadecimal. If Symbols have been defined in the Format Specification, they can also be used for the low and high values.

Data sampling and sorting When Run is pressed, all input channels defined in the Format Specification are sampled. Once acquired, the sampled data is sorted into the buckets of the specified label, and the State Overview display is updated. The acquisition is repeated until Stop is pressed or until a display variable is changed.

Y axis scaling The display builds a vertical histogram where the Y axis represents the relative number of occurrences in each of the buckets. As successive acquisitions are acquired and sorted, the display is constantly re-scaled vertically so that the upper limit of the Y axis represents the largest number of occurrences in any bucket.

The Y axis maximum limit is displayed in Max count.

Total count The Total count field is the total number of states sampled over the entire label range since the measurement was started.

X and O markers Markers can be placed on any bucket to determine the number of occurrences in that bucket. The X Mark count and O Mark count fields display the number of occurrences at the markers. The markers move only on the bucket boundaries.

The range of each bucket can be determined by selecting the X marker or O marker fields and noting the change in the marker value in the pop-up as the marker is moved slowly across the display.

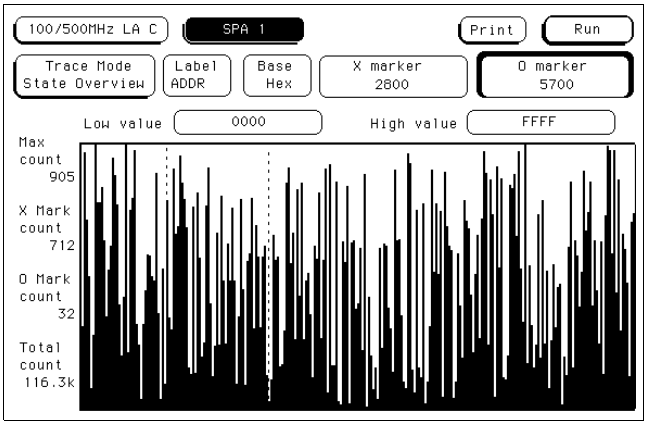
Example

State Overview example

An example of a State Overview measurement is testing for access to a reserved area of memory. In this case, the address bus of the target system would need to be grouped under a single label, such as ADDR. By selecting the ADDR label in State Overview mode, and by defining the full range of the label (Low value = 0000, High value = FFFF with a 16-bit ADDR label), activity over the entire address range can be monitored. Access into reserved memory is easily identified.

By selecting only the range of the reserved area of memory with the Low and High values, the number of address values per bucket is decreased and a more detailed analysis can be performed.

The figure below shows a State Overview display.



SPA State Overview Menu

State Histogram mode

State Histogram mode displays relative activity of ranges of a specified label. The ranges can also be compared to activity on the rest of the label not defined in the ranges. Data qualification is possible with State Histogram, so data can be filtered during acquisition.

Data sampling and sorting When Run is pressed, all input channels defined in the Format Specification are sampled. Once acquired, each sample in the acquisition is compared to each defined range. If the sample value is inclusively within the range and if the range is on, the count for that range is incremented, then the State Histogram display is updated. The acquisition is repeated until Stop is pressed or until a display variable is changed.

The histogram is displayed on a percentage scale, and each bar represents the fraction of all samples in that range. For example, if a bar reaches the 40% value on the display, then the range for that bar contains 40% of all the samples displayed. If the total percentages of all bars equals greater than 100%, then ranges have been overlapped and data has been counted twice.

State Histogram vs. State Overview State Histogram is similar to State Overview, but there are key differences between the two modes. State Overview shows relative distribution of activity over a single contiguous range of a label. State Histogram also allows several non-contiguous ranges of a label to be defined.

State Overview requires minimal setup, and provides a quick overview of system activity. State Histogram requires more setup, but provides greater resolution and measurement flexibility.

State Overview mode does not display data that falls out of the range of its Low and High values. State Histogram, on the other hand, has an "Other States included/excluded" feature that will present a histogram of any activity that does not fall into the defined ranges (see "Other States included/ excluded," later in this section).

State Overview samples and displays all activity on the specified label. But State Histogram allows data qualification so that only activity of interest is sampled and displayed (see "Trace Type: All States vs. Qualified States," later in this section).

Range specifiers A maximum of 11 ranges are available. The ranges are defined by specifying a low and high value on the specified label and by a name you define. The ranges need not be contiguous. If two ranges overlap in any manner, acquired data will be counted in both ranges.

If a range has a low and high value and a name defined, and the range is turned off, it will retain the low and high value and name when turned back on.

User-defined ranges vs. symbols When defining low and high values for the State Histogram ranges, you may use symbols instead of entering discrete values. Symbols can only be used for labels selected in the State Histogram mode if they are defined in the Format Specification, and only if the base in the State Histogram menu is set to Symbol.

Pattern or range symbols defined in the Format Specification can be used to set the low or high value of a range.

Total samples The Total samples field displays the total number of samples in all the displayed ranges. If Other States included is selected, then total samples is the total of all displayed samples plus the other states. If any ranges are overlapped and samples fall in multiple buckets, these samples are only counted once in total samples.

Number of samples per range Displayed next to each bar is a value representing the number of samples for that range. The ratio of these values to total samples determines the relative size of the histograms. These values are updated as the repeated acquisitions are sorted and displayed.

Other States included/excluded Usually the defined ranges will not cover the entire range of the specified label. The Other States included/ excluded field provides an optional histogram showing all activity on the specified label that does not fall within any of the defined ranges. By selecting excluded, the relative activity of only the defined ranges is displayed. If included is selected, the "other" histogram appears under the ranges.

If a range is turned off, any activity in that range is included in Other States. The activity of a turned off range is included in the other range whether included or excluded other states is displayed or not.

Trace Type: All States vs. Qualified States State Histogram mode can qualify data as it is sampled. Qualifying data while sampling allows only data of interest to be stored, while the rest is thrown away.

When Trace Type is set to Qualified States, a new field appears in the upper row of the display. The new field, Specify States, is where the data qualification is defined. The data qualification is not limited only to the label selected in the State Histogram menu. It is defined over all labels in the

Format Specification as a combination of values, in the current base, and don't cares.

For example, a microprocessor target system memory may contain two arrays. In State Histogram, the address ranges of the arrays can be defined and the relative activity in the arrays monitored. But, what if you only want to monitor writes to the array? In this case, you can define the data qualification as "Memory Write" on the STATUS label.

States that do not meet the qualification criteria are not stored by the analyzer, so they are not included in Other States.

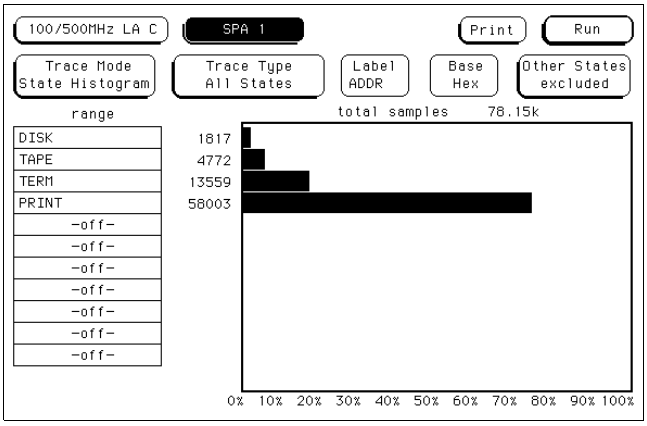
Example

State Histogram example

A computer system has several I/O devices, such as a data terminal, disk drive, tape drive, and printer. Each device has its own service routines stored in memory. The problem is that one or more of the devices is tying up the CPU.

The address bus of the system is monitored using State Histogram to define the memory blocks where the service routines are stored. The histograms quickly show that the print spooler is not working because the printer is constantly interrupting the CPU and is consuming 80% of address bus activity.

The figure below shows a sample State Histogram display.



SPA State Histogram Menu

Time Interval mode

Time Interval mode shows distribution of the execution time of a single event. The event is defined by specifying Start and End conditions as patterns across all labels defined in the Format Specification.

Data sampling and sorting When you press Run, the analyzer samples the target system using the definitions entered in the Format Specification. During acquisition, the state analyzer searches the data for the start and end conditions, and uses the analyzer's time tag feature to time the event. The time durations for each Start/End pair are then sorted into user-definable time interval ranges on the display. The acquisition is repeated until Stop is pressed or until a display variable is changed.

Because time tags are not available in the half-channel mode as specified in the Format menu, time interval mode will not function when half-channel mode is selected.

After the data is sampled, timed, and sorted, the histogram for each time interval range is updated.

If two time intervals are adjacent and have a common boundary (the upper limit of one equals the lower limit of the next), and a sampled time interval falls on the common boundary, the sample will be sorted into the higher time interval.

Start/End conditions Start and end conditions for Time Interval are specified on all labels defined in the Format Specification as a combination of values, in the current base, and don't cares.

If a start or end condition is not found during an acquisition, the histogram will not change. The analyzer will only update when a start and stop event are both found.

Start and end conditions need not be adjacent in the data stream. For example, when the state analyzer sees the specified start condition, it starts the timer. If the start condition occurs again before the end condition occurs, the timer will not be reset.

For measurement purposes, the analyzer measures the time between the first occurrence of the start condition and the first occurrence of the stop condition.

Time Interval ranges A maximum of 8 time interval ranges are available. Each range has a lower and upper limit which can be entered manually. The Auto-range feature will automatically scale the eight

ranges. The minimum allowable limit is 0 ns, the maximum 9,999,999 seconds.

Ranges do not have to be contiguous. However, gaps between ranges increase the risk of missed data. If two ranges overlap, data will be counted in both ranges. This applies to any number of overlapping ranges, or any portions of overlapping ranges. Common boundaries of adjacent ranges are not considered to be overlapped.

A range can be turned off by setting the lower and upper values to zero.

Auto-range The Time Interval ranges can be scaled quickly by selecting "Auto-range." This option requires a global Minimum time and Maximum time for the eight time interval ranges. The eight ranges are then scaled using either a log scale or linear scale.

All the ranges may be quickly initialized to off by selecting Auto-range, setting Minimum time and Maximum time to zero, and performing a linear scale.

The smallest increment allowable using Auto-scale is 10 ns. If the time interval defined by the minimum and maximum times is too small to scale 8 ranges, Auto-range will scale as many as possible and exclude some upper time interval ranges. The maximum resolution of each time interval is 10 ns.

Min, Max, and Avg Time Statistics The Time Interval mode display shows three statistics: Maximum (Max) time, Minimum (Min) time, and Average (Avg) time. These values are displayed whether or not they fall into any of the time interval ranges. Therefore, they are helpful in determining if the appropriate time intervals have been chosen.

The maximum resolution of the statistics is 8 ns.

Total samples Total samples is displayed above the histogram. A sample is defined as one Start/End pair. The Total samples field is not updated until the analyzer's memory is full or until Stop is pressed.

Example

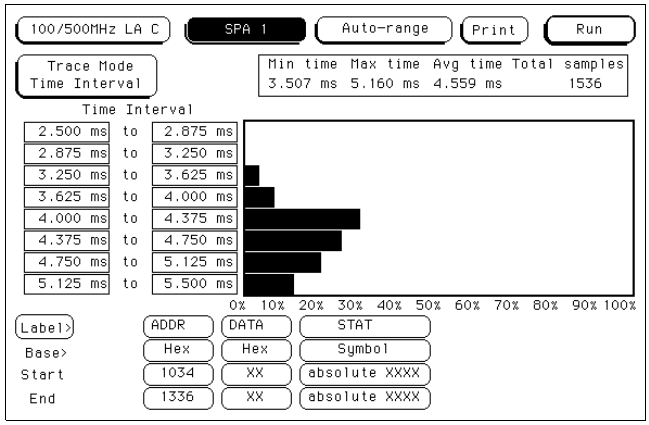
Time Interval example

A team of applications programmers is writing a math package for a spreadsheet. They need to develop standards for the various math functions. Using time interval mode, they can test the execution time of each of the math functions.

For each math function, they enter the starting and ending addresses in the Time Interval menu. They run the math function while monitoring its execution time with their logic analyzer in the Time Interval mode. Using Auto-range, they can quickly vary the time interval ranges for either greater time coverage or greater time resolution.

If the programmers wanted to see the details of the time intervals, they could set up a state analyzer measurement (not using SPA) and capture the activity between the start and stop events. The details could then be viewed in the state listing menu.

The figure below shows a sample Time Interval menu and its display.



SPA Time Interval Menu

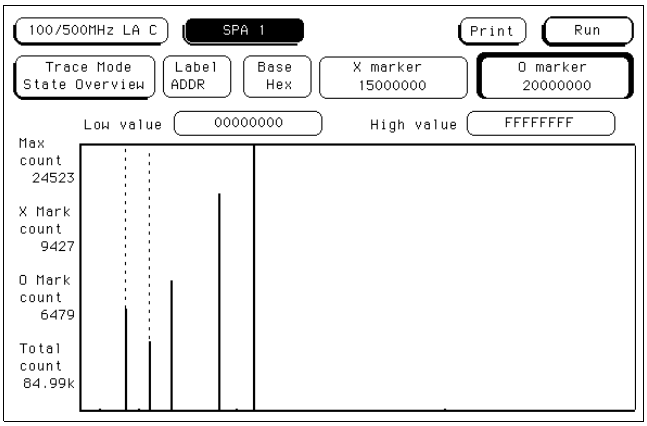
Example

Measurement example using all three trace modes

In a 32-bit microprocessor system, you want to determine how efficiently the CPU is being utilized. Critical questions might be: are any processes consuming excessive processing time, are any processes getting stuck in wait loops, and is the system handling service calls and interrupts efficiently?

You connect the HP logic analyzer to the address bus of your system. In the Format Specification, you define a 32-bit label called ADDR and the state clocking. In many cases, HP provides preprocessors, inverse assemblers and standard configurations for popular microprocessors, and you need not enter the configuration manually or worry about probing issues.

In the State Overview mode, you select the ADDR label and start the acquisition to monitor the entire memory space. After several acquisitions, five areas of relatively high activity begin to build on the histogram. Using the X and O markers to determine the address boundaries of these five regions, you quickly recognize two programs, a delay routine in the operating system kernel, and a keyboard interrupt routine. The figure below shows the State Overview display.

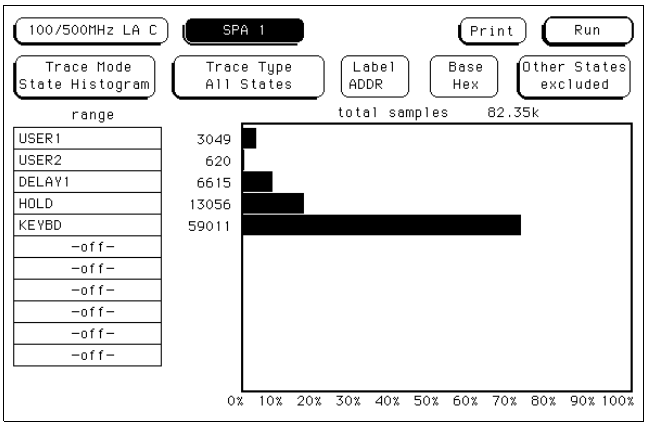


SPA State Overview

Next, you go to the State Histogram menu and enter the names and boundaries of the five routines in the state histogram ranges.

State Histogram then displays the relative activity of the five routines. After several acquisitions, it is apparent that the interrupt routine is being accessed more often than expected.

The figure below shows the State Histogram display for this example.

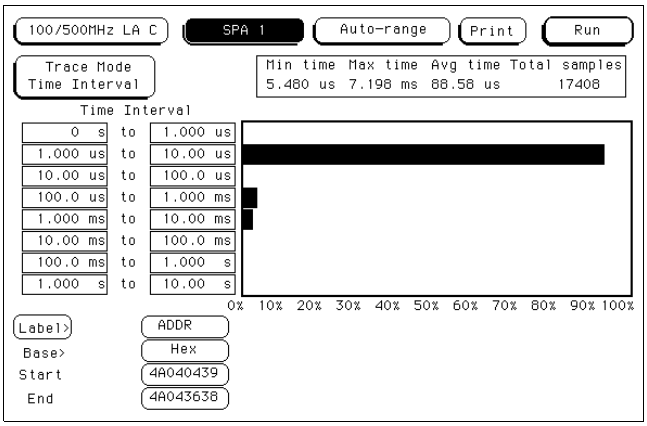


SPA State Histogram

You now go to the Time Interval menu and enter the Start and End conditions for the suspect interrupt routine. Before altering the default Time Interval ranges, you start the acquisition and observe the Maximum (Max), Minimum (Min), and Average (Avg) times. From these values, the typical execution times of the interrupt are apparent, and provide good starting values for the Time Interval ranges using Auto-range. From the Max time, it is apparent that the interrupt routine is having problems.

Running the acquisition again, you discover that the interrupt usually takes the expected 8 microseconds, but occasionally it takes as long as 8 milliseconds. After experimenting with the target system while monitoring the interrupt with Time Interval mode, a faulty key on the keyboard is discovered. The key is bouncing excessively, resulting in an extended interrupt routine call.

The figure on the next page shows the Time Interval display for this example.



SPA Time Interval

Using State Overview, State Histogram, and Time Interval

This section explains how to select the display fields, set up the logic analyzer and use the State Overview, State Histogram and Time Interval modes of SPA.

Setting up the logic analyzer

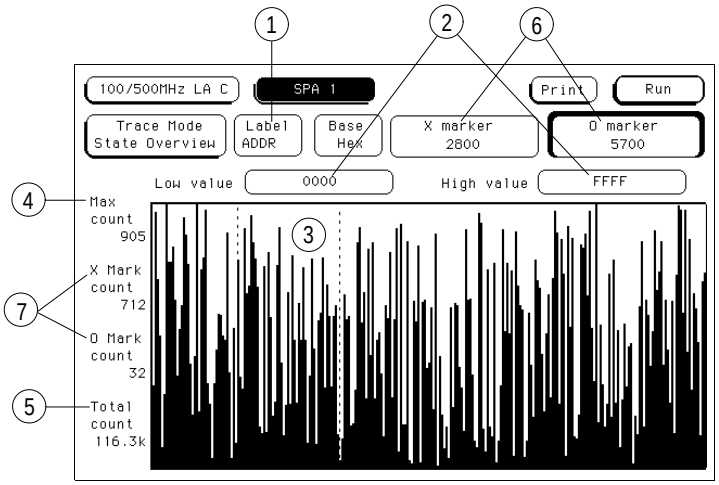
This section assumes you have defined the Format and have connected the logic analyzer probes to the target system. For complete details on these topics, refer to the appropriate reference section for your analyzer.

For a detailed description of State Overview, State Histogram, and Time Interval mode measurement processes, refer to the previous section, "SPA measurement processes."

Using State Overview mode

Choosing a label to monitor To specify a label to monitor, select the "Label" field in the State Overview menu (item 1 in the figure on the next page). The pop-up shows a list of all the labels defined in the Format Specification. From this list, choose the label you want to monitor.

Changing from one label to another will erase the display setup for the first label. If you want to change to a different label, but don't want to lose the setup for the current one, first save the current one to disk or print it.



SPA State Overview Menu with Fields Called Out

Specifying Low and High values The range of the X axis is determined by the Low value and High value fields (item 2 in figure above). To change the X axis range, select the Low value or High value fields and enter new limits. The range you specified will then be divided among the 256 available buckets along the X axis (unless the range is less than 256 or the histogram frame is truncated due to bucket range round-off).

For example, you might set the low and high values so that the range is 1100. 1100 divided by 256 is 4.29. This will be rounded up to 5, and each bucket will have a range of 5. Because 1100 divided by 5 is 220, the histogram frame will be truncated at the right because the X axis will have only 220 of the 256 buckets.

The default high and low values represent the full range of the label you chose. Before changing these values, you may want to run the acquisition and acquire some data to view activity over the entire range of the label. You can then zoom in on areas of interest.

You can enter low and high values in binary, octal, decimal, hexadecimal, ASCII, or symbol.

Interpreting the histogram display Press the blue shift key and Run to start the State Overview acquisition. As the data is sampled and sorted, the buckets along the X axis will accumulate (item 3 in the figure on the previous page). The relative size of the vertical bars show the distribution of activity on the label you chose. The analyzer will continue to sample, sort the data, and update the display until you press Stop or until you change a display variable.

Max count (item 4 in the figure on the previous page) represents the current upper limit of the Y axis for the bucket with the greatest number of data samples. Max count for the limit of the Y axis will increase as the buckets fill with samples.

Read Total count (item 5 in the figure on the previous page) to find the total number of samples taken over the specified range of the label. This is not affected by the low and high values.

Using the markers To find the number of data samples in any bucket, select the X marker or O marker field (item 6 in the figure on the previous page). Turn the knob to move the marker to the area of interest. Read the X Mark count or O Mark count values to determine the number of samples in the current bucket (item 7 in the figure on the previous page).

As you move either marker across the display, the value in the X Marker or O Marker pop-up will change. The amount of change of the marker's value represents the size of the bucket.

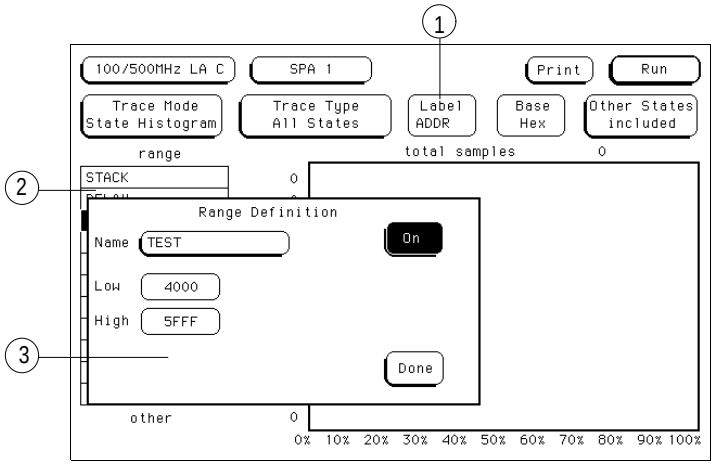
Zooming in on an area of interest When viewing the State Overview display, you may see areas of high activity and areas of little or no activity. To zoom in on one of these areas for more resolution, put the X and O markers on the boundaries of the area, then adjust the low and high values to match the X and O marker positions.

Using State Histogram mode

Choosing a label to monitor To specify a label to monitor, select the Label field in the State Histogram display (item 1 in the figure below). In the pop-up, you will see a list of all the labels defined in the Format specification. From this list, choose the label you want to monitor.

> Changing from one label to another will erase the display setup for the first label. If you want to change to a different label, but do not want to lose the setup for the current one, save the current one to a disk.

Defining the ranges To define a range on the specified label, select one of the 11 range fields (item 2 in the figure below). When you select one of the 11 ranges, you will see the Range Definition pop-up (item 3 in the figure below). This pop-up has fields where you enter the low and high value, a name for the range, and whether the range is on or off.



SPA State Histogram Menu with Fields Called Out

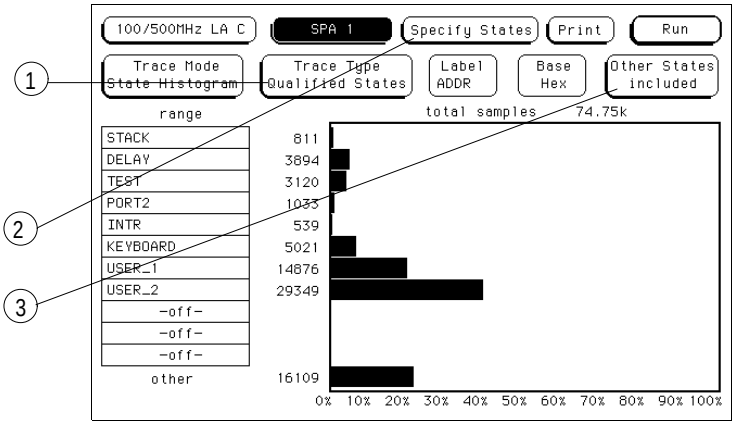
Using symbols for ranges In the Format menu, you can define symbols for any available label. The symbols can be defined as Pattern Symbols or Range Symbols. For complete information on defining and using symbols, see "Symbols field" in Chapter 8.

If you set the base field in the State Histogram display to Symbol, you can use any defined range or pattern symbol to set the lower and upper values of the ranges.

Tracing All States vs. Qualified States You can qualify the data sampled and sorted in the State Histogram by selecting the Trace Type field and setting it to Qualified States (item 1 in the figure below). This creates a new field at the top of the display called "Specify States."

Select Specify States (item 2 in the figure below) and you will see a pop-up that contains a pattern field for every label defined in the Format Specification. Use the pattern fields to define the data qualification.

For example, in the State Histogram you may want to monitor the address bus of a microprocessor system to examine memory activity. But, you may want to monitor only writes to memory. In the Specify States pop-up, you can tell the analyzer to sample only memory writes by entering under the STATUS label the bit pattern or symbol that corresponds to memory writes.



SPA State Histogram Menu with Fields Called Out

Interpreting the histogram display Press the blue shift key and Run to start the State Histogram acquisition. The relative activity over the ranges you defined is displayed as histograms (see the figure on the previous page). The total samples field shows the total number of data samples displayed in all of the ranges. The number of samples for each range is displayed to the left of each histogram.

The percentage amounts of the histograms total 100% (note the scale at the bottom of the display). If they add up to more than 100%, you have overlapped two or more ranges, and the data samples are being counted in multiple ranges.

The analyzer will continue to sample, sort the data, and update the display until you press Stop or change a display variable.

Other States included/excluded The histograms show the relative distribution of activity over the ranges you have defined. In most cases, the ranges will not cover the full range of the label you chose to monitor.

To view the activity over the entire range of the label, including activity not covered by the ranges, select the Other States field and change it to included (item 3 in the figure on the previous page). Another histogram bar called "other" will appear at the bottom of the display. This will show activity not covered by the ranges. You can toggle included/excluded if the analyzer is stopped or if it is running because it only affects the display and not the accumulated data that has been acquired.

Note that changing between included and excluded changes the absolute sizes of the histograms. Unless you have defined overlapping ranges, the total percentage size of the all the range histograms plus the histogram for other should equal 100%.

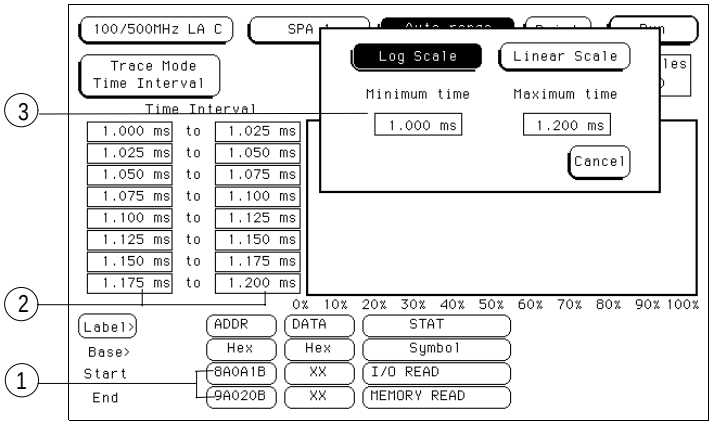
Using Time Interval mode

Use Time Interval mode to determine the distribution of time between two specific events. The state analyzer uses the time tag feature to time the event; thus, in Time Interval mode, the minimum state clock period is 10 ns.

Specifying an event To use Time Interval mode, you must define an event that you want timed. At the bottom of the display, note the Start and End fields (item 1 in the figure below). To define an event, select the appropriate labels in the Start and End fields to define the boundaries.

For example, start and end might be the beginning and ending addresses of a subroutine stored in memory. If you are timing a counter period, start and end might be the initial and final count values.

Note that in start and end, you are not limited to a single label. You define the event over all available labels as patterns including don't cares. Be sure that the start and end conditions actually occur in the target system or the analyzer will not find the timing reference points and will not make the time interval measurement. You may want to use the state analyzer (not SPA) to verify that the Start and Stop events actually occur.



SPA Time Interval Menu with Fields Called Out

For measurement purposes, the analyzer measures the time between the first occurrence of the Start condition and the first occurrence of the Stop condition.

Defining the Time Interval ranges Before changing the ranges from their default values, you may want to press Run and acquire some data. From this initial run, the Maximum (Max), Minimum (Min), and Average (Avg) statistics on the display will help you choose the appropriate set of Time Interval ranges.

To define the ranges, select the fields for the lower and upper limits (item 2 in the figure on the previous page) and enter the limits of the range. The ranges do not need to be contiguous, but if you leave gaps between the ranges, critical data may be missed. Also, if you overlap ranges, data may be counted multiple times and present a misleading histogram.

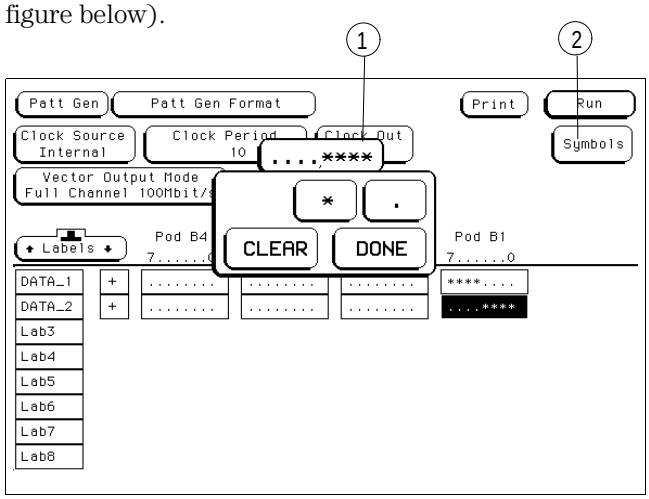
Using Auto-range To quickly set up all 8 time interval ranges, select the Auto-range field. Enter the minimum time and maximum time for all 8 ranges combined. Then, when you select Log Scale or Linear Scale, all 8 ranges will be scaled accordingly between the Minimum and Maximum times. See item 3 in the figure on the previous page for the Auto-range pop-up. Common boundaries of adjacent ranges are not considered overlapped. Values that fall on the common boundary will be included in the highest range.

A fast way to set up the Time Interval display is to define your Start and End events and select Run using the default ranges. Select Repetitive Run mode. After accumulating data for a while, press Stop. Then select Auto-range and enter the Min time and Max time display statistics in the Auto-range Minimum time and Maximum time fields. When you select Log Scale or Linear Scale, the ranges will be defined automatically.

Interpreting the histogram display As the analyzer samples the data, it searches for Start/End event pairs. One event pair is considered one sample. The time value for each event pair is compared to each defined time interval range. The range's count is incremented if the time value falls within that range.

The analyzer continues to search for Start/End event pairs until you press Stop or change a display variable. The distribution of the events' time duration is displayed as histograms.

The Max time, Min time, and Avg time statistics give you useful statistics for the event you defined no matter what ranges you've set up (item 1 in the figure below).



SPA Time Interval Menu with Statistics Called Out

The Total samples field shows the number of Start/End event pairs found by the analyzer, whether they are covered by the ranges or not (item 2 in the figure above).

Using SPA with other features

Programming with SPA

SPA is programmable. Refer to the *HP 1660C/CS/CP-Series Logic Analyzers Programmer's Guide* for SPA commands. The Programmer's Guide is available as an option with the logic analyzer. Contact your HP Sales Office for more information.

Changing between SPA and a State/Timing Analyzer

If you have configured a state or timing analyzer in the logic analyzer, you can quickly change to SPA, or from SPA to a state or timing analyzer. You can use the same Format Specification in your SPA measurements as you did in your state or timing analysis measurements.

To change between a state analyzer and SPA, go to the Analyzer Configuration menu, select the Type field, and select SPA from the list.

When SPA is selected, a separate trace specification definition is used. Even though the Qualified State Histogram and Time Interval modes use the same pattern recognizers as SPA, the SPA definitions are kept separate from those entered in the state or timing analyzer mode. As a result, switching between SPA and state or timing recovers the user's original pattern recognizers for the selected mode.

Any Symbols in the Format Specification will also carry over to SPA.

Using SPA in Group Runs

In the HP 16500A Logic Analysis System, you can define an intermodule sequence using various combinations of modules and run it singly or repetitively. Similarly, the HP 1660C-series logic analyzers allow you to set up group runs using the Arming Control field of the other machine's Trigger menu.

By its statistical nature, SPA runs best as a repetitive measurement system. Therefore, if you include SPA in a Group Run, it will execute and update the SPA displays, but the data may not be acquired in a statistically random-repetitive fashion. It may not represent a true statistical analysis of your target system.

Another way to make SPA measurements in conjunction with other analysis is to run SPA independently (do not include it in the Group Run), and set up the other machines as you normally would. In this way, SPA will provide a truer statistical analysis of your target system.

Concepts

Concepts

Understanding how the analyzer does its job will help you use it more effectively and minimize measurement problems. This chapter explains the structure of the file system, the details of transitional timing mode, the general operation of the trigger sequence, and the details of the hardware.

The File System

The HP 1660CP-series logic analyzers have a complex internal file system. Many of the file attributes are only accessible over a LAN connection. From the logic analyzer's front panel, the only parts of the file system you can examine are the hard disk drive and the flexible disk drive. The hard disk drive contains the /SYSTEM directory with the X Window fonts and some example files, and also whatever other files and directories you have created on it. The flexible disk drive directory contains whatever files are on the disk in the disk drive.

See Also

The *LAN User's Guide* for more information on the LAN-accessible portions of the file system.

Directories

Hard disk drive

When you receive the logic analyzer, the hard disk drive is already DOS-formatted. The factory also creates a directory on the hard disk drive named "/SYSTEM". The /SYSTEM directory is intended to store system software such as backup copies of the operating system files and the performance verification files. When you receive your logic analyzer, the /SYSTEM directory already contains two X Window font files and several files containing examples.

The files on the hard disk drive are not essential to the logic analyzer's correct operation. However, you can store important files such as optional software, autoload files, configurations, and software backups here. You can configure the logic analyzer to Autoload files from the hard disk at power-up.

When the logic analyzer searches for autoload files and software options, it first looks in the flexible disk drive. If the flexible disk drive contains an autoload file and two software options, the analyzer does not check the hard disk drive. If some of these were not found, the analyzer next checks the hard drive's /SYSTEM directory.

You can manually copy files, such as performance verification files, to the /SYSTEM directory, but they will not necessarily be installed when the analyzer powers up. To automatically load software, follow the installation instructions provided with the software. It will change the power-up sequence to include the software option and also copy the files to the /SYSTEM directory.

Flexible disk drive

The flexible disk drive reads 3.5-inch flexible disks in both DOS and LIF format. If a disk is in the drive when the analyzer is turned on, the analyzer checks the disk for software and autoload files. If these files are found, they are loaded into the analyzer.

File types

There are six common file types on the HP 1660CP-series logic analyzer. In addition, there are six common filename endings. The X Window font files and the example files in the /SYSTEM directory do not use these file types.

Standard file types

The file type is shown in a small display box centered on the line above the file listings.

autoload_file indicates the file, almost always named AUTOLOAD, is an autoload file. The file description indicates if the autoload file is enabled or disabled, and the file it autoloads. Autoload files are created by executing "Autoload" in the System Disk menu.

166xan_config indicates the file is an analyzer configuration. These files are created by executing "Store Analyzer" or "Store All" in the System Disk menu.

16[6/7]x_cnfg indicates the file is a system configuration. These files are created by executing "Store System" or "Store All" in the System Disk menu.

DOS indicates the file is in DOS format. It might be a screenshot or a file created on a PC and copied to the disk. These files are not loadable.

directory indicates the file is a directory and that you can change to that directory. Other files are within it.

16[6/7]x_opt indicates the file is software that can be used with either the HP 1660 or HP 1670 family of logic analyzers.

16522_cnfg indicates that the file is a pattern generator configuration. These files are created by executing "Store Patt Gen" in the System Disk menu.

Filename endings

Filename endings are not restricted to certain types. These descriptions are just general guidelines. In addition, other tools you use with the logic analyzer will likely have their own set of filename endings.

[none] Of the common file types you can create using the logic analyzer, only the ASCII listings do not have a default ending. If you supply one in the Print to Disk filename field, that ending will be used, but no ending is automatically appended as with other filenames.

Three other types of files commonly do not have a default ending: directories, software, and autoload files. Check the file type field to be sure what type of file you are selecting.

._A This ending is appended to analyzer configuration files created with the Store operation from the System Disk menu.

._B This ending is appended to pattern generator configuration files created with the Store operation from the System Disk menu.

._ _ This ending is appended to system configuration files created with the Store operation from the System Disk menu.

.TIF This ending is appended to TIFF version 5.0-format screenshots created with the Print to Disk function.

.EPS This ending is appended to EPS-format screenshots created with the Print to Disk function.

.PCX This ending is appended to PCX-format screenshots created with the Print to Disk function.

Transitional Mode Theory

In Transitional acquisition mode, the timing analyzer samples data at regular intervals, but only stores data when there is a transition between logic levels on currently assigned bits of a pod pair. Each time a level transition occurs on any of the bits, all bits of the pod pair are stored. A time tag is stored with each stored data sample so the measurement can be reconstructed and displayed later.

One issue when using transitional timing is how many transitions can be stored. The number depends on the mode and frequency of transition occurrence. The following overview explains the number of transitions stored for each transitional timing mode and why.

125-MHz Transitional mode

When the timing analyzer runs in the 125-MHz mode, it operates like the state analyzer with Count Time turned on, the exceptions being that the store qualification comes from transition detectors instead of the sequencer and that the analyzer uses an internal clock.

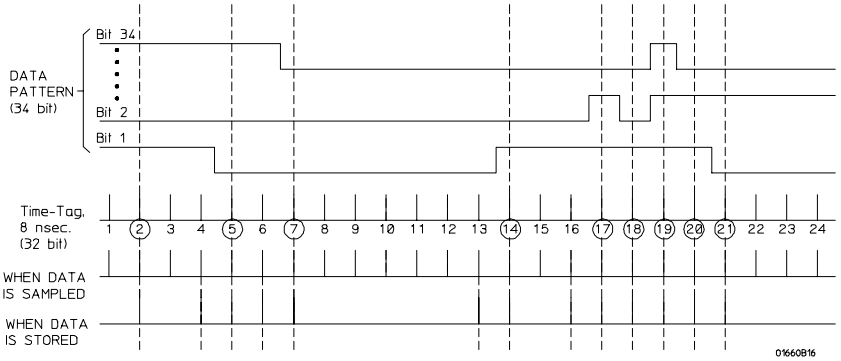
With 4 K of memory per channel and Count Time selected, the analyzer uses half its memory (2 K) to store time tags. Because each pod pair must store transitions at its own rate, each pod pair must store its own set of time tags. This is why you do not have the option of using a free pod to retain full memory as you have in the normal state mode.

When a transition is detected after a sample with no detected transition, both samples are stored. If the next sample also indicates a transition, only one sample is stored. If the next sample does not indicate a transition, no sample is stored this time and the next transition again stores two samples.

Minimum transitions stored

Sometimes transitions occur at a relatively slow rate, slow enough to ensure at least one sample with no transitions between the samples with transitions. This is illustrated in the figure on the next page with time tags 2, 5, 7, and 14. When transitions happen at this rate, two cycles are stored for every transition. This means that with 2 K of memory, 1 K of transitions are stored,

or because transitions take one sample space, 1024 transitions are stored. Subtract 1 for the starting point and you have a minimum of 1023 stored transitions.



Storing Time Tags and Transitions

Maximum transitions stored

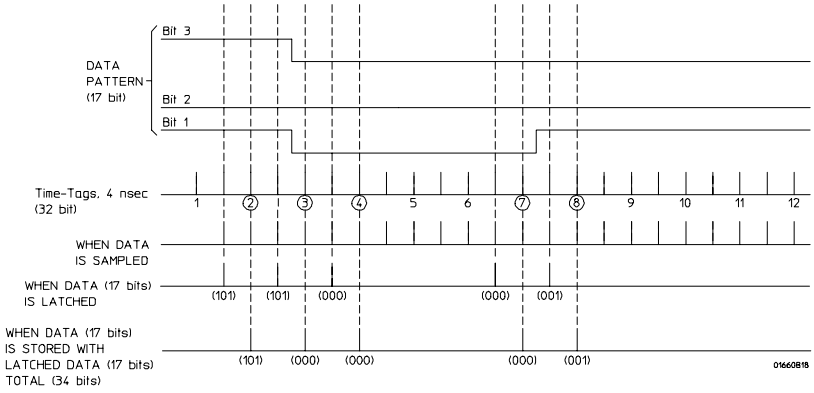
If transitions occur at a fast rate, such that there is a transition at each sample point, only one sample is stored for each transition as shown by time tags 17 through 21 above. If this continues for the entire trace, the number of transitions stored is 2 K divided by 1 sample per transition. Again, you must subtract the starting point sample, yielding a maximum of 2047 stored transitions.

In most cases a transitional timing trace is stored by a mixture of the minimum and maximum cases. Therefore, the actual number of transitions stored will be between 1023 and 2047.

250-MHz Transitional mode

Transitional timing running at 250 MHz is the same as the 125-MHz mode, except that two single-pod data samples (17 bits x 2 = 34 bits) are stored instead of one full-pod-pair data sample (34 bits). This is because in half-channel mode, data is multiplexed into the pipeline in two 17-bit samples. The first 17-bit sample is latched, and at the next 17-bit sample both samples are sent down the pipeline.

This operation keeps the pipeline frequency at 125 MHz, which means the transition detector still looks at a full 34 bits. Essentially, the transition detector is looking at two samples at a time instead of one. In the 250-MHz mode, between 682 and 4094 transitions are stored.



Minimum Transitions Stored

Minimum transitions stored

The figure above shows what data is stored from a data stream with transitions that occur at a slow rate (more than 24 ns apart).

As shown, transitions are stored in two different ways, depending strictly on chance. Remember that the transition detector only looks at the full 34 bits while the data is stored as two 17-bit samples. So, the transition detector will not see time tag 3 (101/000) as a transition. However, when the detector compares the transition to time tags 2 (101/101) or 4 (000/000), it sees a difference and detects them as transitions. For this first set of time tags, the transition detector sees more transitions than are really there. This causes the analyzer to store 6 samples per transition (three 34-bit sample pairs), instead of just two, as in the 125-MHz mode. If all of the transitions will be stored in this way throughout the trace, the minimum number of stored transitions is 682 (4096/6).

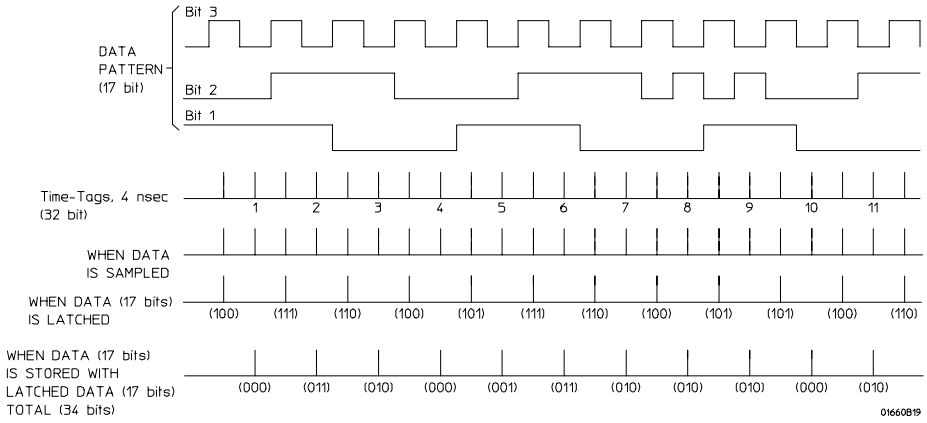
However, as you see with time tags 7 (000/000) and 8 (001/001), transitions can fall between the pairs of samples. When this happens, only one transition is detected and only 4 samples (two sample pairs) are stored. If all transitions will be stored in this way, 1023 (4096/4) transitions are stored.

From run to run, the actual number of transitions stored for transitions that occur at a slower rate will fall between these two numbers, based on the

probability of a transition falling between a sample pair or falling within a sample pair.

Maximum transitions stored

The following example shows the case where the transitions are occurring at a 4-ns rate:



Maximum Transitions Stored

In this case, transitions are being detected with each sample so all samples are stored. This situation also means each sample pair contains a transition. For example, time tag 1 (100/000) contains a transition and is different from time tag 2 (111/011), which also contains a transition. The difference between the sample pairs of time tag 1 and time tag 2 will trigger the transition detector.

If this were to continue throughout the trace, the analyzer would store a single sample for the entire 4 K of memory, or 4096 samples. Again, subtract one for the initial sample which is not a transition for a final total of 4095 transitions recorded. As with the 125-MHz mode, the actual number of transitions stored will fall somewhere between 682 and 4095, depending on the frequency of transitions.

Other transitional timing considerations

Pod pairs are independent In single run mode, each pod pair runs independently. This means when one pod pair fills its trace buffer it will not shut the others down. If you have a pod pair with enabled data lines and no transitions on its lines, you get a message "Storing transitions after trigger for pods nn/nn." In repetitive run mode, a full pod pair waits 2 seconds, then halts all other pod pairs.

Increasing duration of storage In the 125-MHz mode, a transition on any one of the 34 bits in a sample (if they are all turned on) will cause storage. Reducing the number of bits that are turned on for any one pod pair will more than likely increase data storage time.

Separating data lines which contain frequent transitions from lines with less frequent transitions also helps. When doing this, be sure to cross pod pair boundaries. It does not help to move fast lines from pod 1 to pod 2; fast lines must be moved to pod 3, a different pod pair.

In the 250-MHz mode, a transition on any one of 17 bits (half-channel) each sample (if they are all turned on) will cause storage.

Invalid data The analyzer only looks for transitions on data lines that are turned on. Data lines that are turned off store data, but only when one of the lines that is turned on transitions. If the data line is turned on after a run, you would see data, but it is unlikely that every transition that occurred was captured.

The Trigger Sequence

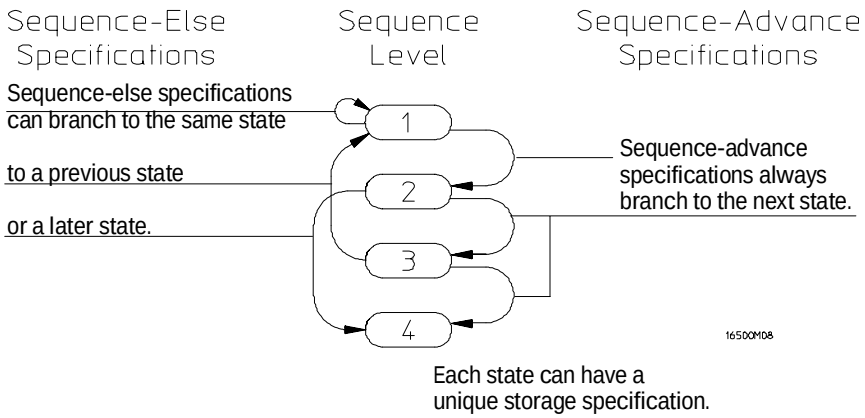
HP 1660CP-series logic analyzers have triggering and data storage features that allow you to capture only the system activity of interest. Understanding how these features work will help you set up analyzer trigger specifications that satisfy your measurement needs.

In both the state and timing analyzers, the trigger sequence acts as a filtering mechanism, with a minimum of two steps and a maximum of twelve steps in the state analyzer and ten steps in the timing analyzer. Some trigger macros may use more than one step. The steps are the sequence level specifications. The analyzer searches for a trigger sequence by matching input values on the pods to branch conditions, which control transitions between sequence levels. You can insert or delete levels to make the trigger sequence as simple or complex as is needed for your application.

Trigger sequence specification

See the following figure, which shows a sequence specification with four levels. To define the trigger sequence, you specify sequence-advance, sequence-else, storage, and trigger-on specifications.

Each level except the last has two branch conditions, the sequence-advance and sequence-else specification. The storage specification indicates whether data should be stored or not while the logic analyzer is at that sequence level. (The trigger-on specification is a special sequence-advance specification that is described in the section "Trigger on specification.")



State Analyzer Sequence with Four States

Sequence-advance specification The sequence-advance branch, sometimes called the "if" branch or primary branch, always branches to the next level. You can specify the following kinds of sequence-advance specifications:

```
Find (or Then find) "<TERM>" <OCCURS> time(s)

Find (or Then find) "<TERM>" <TIME PERIOD>
```

If the <TERM> is found <OCCURS> number of times or the <TERM> remains stable for <TIME PERIOD>, the analyzer advances to the next sequence level.

Sequence-else specification The sequence-else branch, sometimes called the "else if" branch or secondary branch, may branch to any other state, including the current state, a previous state, or a later state. The sequence-else specification looks like the following:

```
Else on "<TERM>" go to level <sequence level>
```

If the Sequence-Else specification is satisfied before the sequence-advance specification, the sequencer goes to <sequence level>.

The last state may only have a sequence-else branch specification, which may branch to the same state or a prior state.

Storage specification In each state, a storage specification determines the data stored by the analyzer while it is searching for the sequence-advance, sequence-else, and trigger specifications. Storage specifications are defined using the same pattern, range, and timer resources available for defining branching specifications.

```
While storing "anystate", "no state", or "<TERM>"
```

Note that if you specify "no state," the analyzer still stores sequence-advance terms and TRIGGER terms unless you also set Branches Taken Not Stored in Acquisition Control in the Analyzer Trigger menu.

Trigger on specification If there are branch and storage specifications for each sequence level, what does the trigger term mean? The trigger term is a special sequence-advance specification in that, when found, it locks the contents of analyzer acquisition memory. The trigger can be positioned at the beginning, middle, or end of acquisition memory.

The trigger specification can look like the following:

```
TRIGGER on "<TERM>" <OCCURS> times
```

```
TRIGGER on "<TERM>" <TIME PERIOD>
```

If the trigger term is found <OCCURS> times, or if the trigger term remains stable for <TIME PERIOD>, the trigger is captured in memory. Then the analyzer advances to the next sequence level. If you want to capture activity after the trigger is captured, define an additional sequence level and specify the desired storage qualification for post-trigger activity (for example, store anystate).

Analyzer resources

The sequence-advance, sequence-else, storage, and trigger-on specifications are set by a combination of a maximum of 10 pattern terms, 2 range terms, 2 timers, and 2 edge terms (for the timing analyzer only). A resource can only be assigned to one analyzer at a time.

10 pattern terms The pattern terms, a through j, represent single states to be found on labeled sets of bits. For example, you could have an address on the address bits or a status on the status bits, or both the address and status occurring together. Pattern terms AND conditions occurring on separate labels.

2 timers You can start, stop, continue, or pause the timers upon entry to a sequence state, then use a comparison of current timer value against a preset value to determine whether to branch to another state.

2 range terms The range terms, Range1 and Range2, represent ranges of values to be found on labeled sets of bits. For example, you could have a range of addresses to be found on the address bus or a range of data values to be found on the data bus. Range terms are satisfied by any value within the range for "In_Range," and any value outside the range for "Out_Range."

2 edge terms (timing analyzer only) The edge terms, Edge1 and Edge2, represent edges. The edge terms can be set to catch glitches even when the timing analyzer is not in glitch mode. When an edge term comprises more than one channel, it ORs the channel conditions together and any of the specified transitions satisfy the term.

You can combine the pattern terms and range terms with logical operators to form complex pattern expressions in the sequence-advance, sequence-else, and TRIGGER on specifications.

For example,

```
Find "(<TERM1>•<TERM2>) + (<TERM3> • <TERM4>)"
```

Where <TERM> can be a single value on a set of labels, any value within a range of values on a set of labels, or a glitch or edge transition on a bit or set of bits.

Limitations affecting use of analyzer resources There are limitations on the way resources can be combined to form complex pattern expressions. Resources are combined in a four-level hierarchy. First, resources are divided into two groups. The groups can be combined with AND or OR. Second, within these groups, resources are combined into pairs. Pairs can also be logically combined using AND or OR. Third, individual resources are combined into pairs using AND, NAND, OR, NOR, XOR, and NXOR. Fourth, individual resources may be included or excluded from participating in a pattern expression. You can also include the logical negation of the resource. Fifth, the timing terms are not available in the first sequence level.

The following table shows how resources are divided in the logic analyzer. Remember that some resources may not be available, depending on the analyzer configuration. For example, if you are using the analyzer as a state analyzer, the Edge1 and Edge2 resources are not available, and only one analyzer may use a resource at a time.

Table 9-1 Resource Combination Hierarchy

Group	Pair	Resource Operation	Resource	Pair Links	Group Link
Group 1	Pair 1	Off, On, Negate	a	Combine resources within pairs using AND, NAND, OR, NOR, XNOR	Combine pairs within groups or group 1 and group 2 using AND or OR
		Off, On, Negate	b		
	Pair 2	Off, On, Negate	c		
		Off, In Range, Out of Range	Range 1		
	Pair 3	Off, On, Negate	d		
		Off, On, Negate	Edge 1		
	Pair 4	Off, On, Negate	e		
		Off, <, >	Timer 1		
Group 2	Pair 1	Off, On, Negate	f	Combine resources within pairs using AND, NAND, OR, NOR, XNOR	
		Off, On, Negate	g		
	Pair 2	Off, On, Negate	h		
		Off, In Range, Out of Range	Range 2		
	Pair 3	Off, On, Negate	i		
		Off, On, Negate	Edge 2		
	Pair 4	Off, On, Negate	j		
		Off, <, >	Timer 2		

For example, the following combinations are valid combinations for the analyzer:

```
(a+b) • (In_Range2 + Timer2 > 400 ns)
```

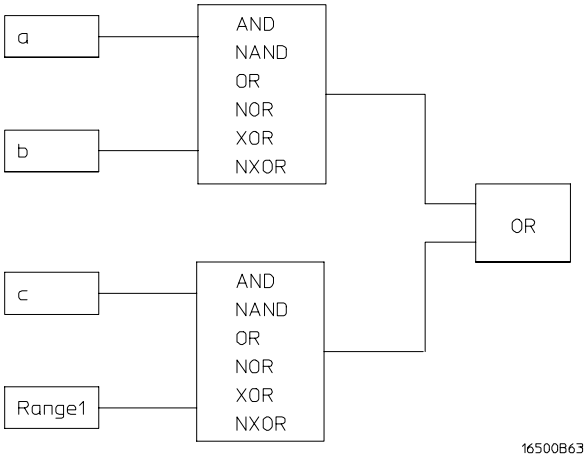
```
(c • Out_Range1) + (f xor g)
```

The following combinations are not valid, because resources cross pair boundaries:

```
a xor c
```

```
(d + Timer1 < 400 ns) • Edge1
```

The first example shows that a and c cannot be combined at the first level. The following figure shows the possible combinations of the a, b, c and Range1 terms:



Combining a, b, c, and Range1 Terms

The following combination is not valid because pairs cross group boundaries:

```
((a+b) + (h • In_Range2)) • (j xor Timer2 > 400 ns)
```

Note that although the analyzer interface will not let you enter invalid combinations, you need to be aware of what combinations are legal, so that you can make the desired measurement.

Another limitation is that the analyzer cannot handle ranging for input pods that are assigned to different pod pairs. For example, if you need to define a 32-bit range term, you must do it using pods 1/2, 3/4, or 5/6. Trying to define a range across pods 2/3, 4/5, or 1/6 will not work.

Timing analyzer

When you configure a timing analyzer, the trigger sequence follows the general outlines given previously. The trigger sequence of the timing analyzer differs from the state analyzer in the following ways:

- There are 10 levels available to build a trigger.
- The trigger term is always the last step.
- The timing analyzer has two additional resources, Edge1 and Edge2.
- Edge1 and Edge2 recognize occurrences of a glitch, rising edge, falling edge, either edge, or no edge on a bit or ORed set of bits.

State analyzer

When you configure a state analyzer, the trigger sequence follows the general outlines given previously. The trigger sequence of the state analyzer differs from the timing analyzer in the following ways:

- There are 12 levels available to build a trigger.
- The trigger term is never the last step.
- The state analyzer cannot use Edge1 and Edge2.

Configuration Translation Between HP Logic Analyzers

Analyzer configuration files cannot be transferred directly from one type of analyzer to another because each analyzer has internal architectural differences, reflected in the number of pods, clock configurations, trigger sequence features, analyzer resources, and so on. To help you move configuration files from one analyzer to another, most HP logic analyzers support automatic translation of analyzer configurations. The HP 1660CP-series logic analyzer can translate configuration files from the following common analyzer models:

- HP 16510
- HP 16511
- HP 16540
- HP 16541
- HP 16550
- HP 1660A

If you save an analyzer configuration from one model of analyzer, then load that configuration into a model that supports configuration translation and was released after the original analyzer, the translator will adjust the configuration as required to account for differences between the models.

The configuration translator needs to account for many aspects of the analyzer architecture. Some of the considerations are as follows:

- When a range term is split across multiple pods, the term must span adjacent odd/even pairs, starting with 1. Thus, terms could span pods 1 and 2, 3 and 4, 5 and 6, or 7 and 8, but not 2 and 3. Again, the translator may display messages asking you to reconnect cables in a different configuration.
- When loading a configuration into an analyzer with fewer pods than the one on which the configuration was saved, the translator must remove pod assignments. Which pods are removed from the configuration will depend on the widths of each pod in the original analyzer and new analyzer.

The configuration translation also needs to account for many differences in the format and trace menus between the analyzers, including label names, polarities, thresholds, symbols, clocking, number of sequence levels, branch conditions, and patterns, among others.

To ensure that trace measurements act as expected when you move configuration files from one analyzer to another, follow these recommendations:

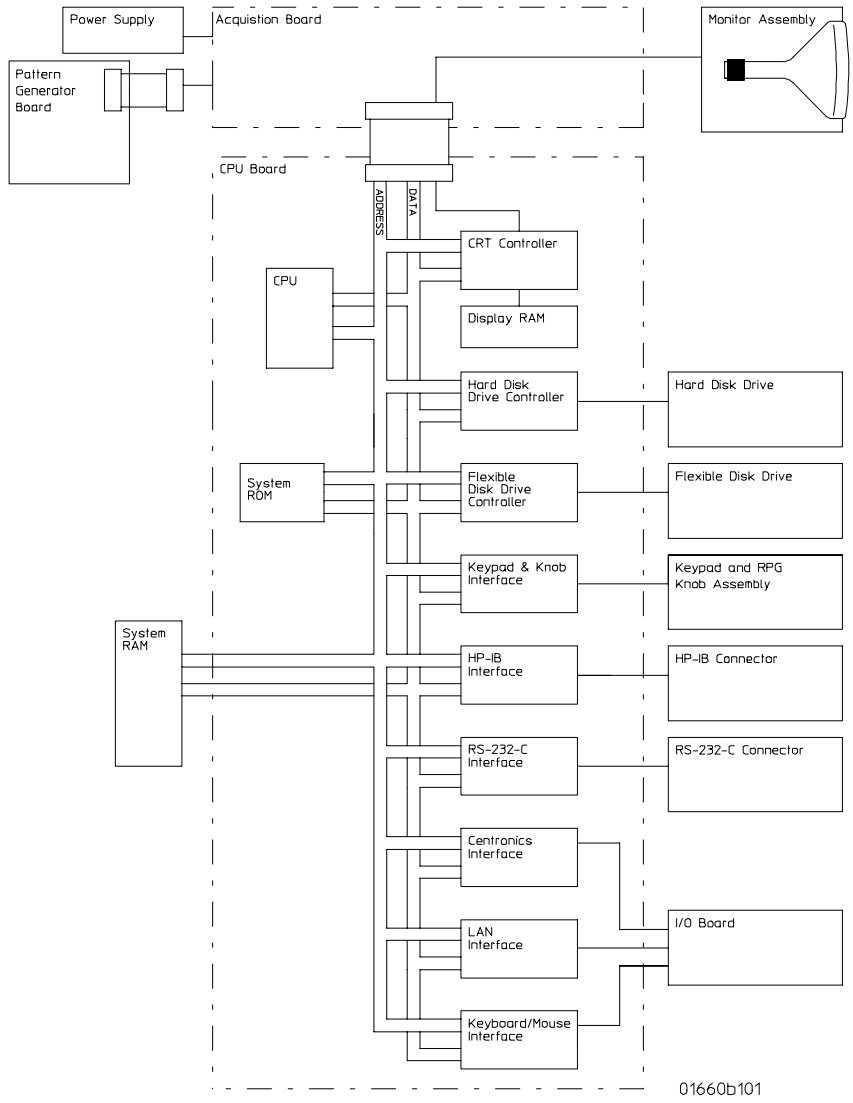
- Ensure that the analyzer pods are hooked up as required by the configuration translation and the new analyzer. The onscreen messages given by the translator will help you identify which analyzer pods must be swapped. If you are using an HP preprocessor, the *Preprocessor User's Guide* may contain information showing the cable connections for different analyzer models.
- Review all trace format and trigger menu settings to verify that they will meet your measurement requirements. You should check label assignments, channel masks, pattern and range definitions, sequencer setup, and general analyzer configuration (which pods are mapped to each analyzer).

When you move a configuration file from one analyzer to another, the trace data from previous measurements is not moved. If you need to store trace data for future reference, see "To save a trace list in ASCII format" in Chapter 7.

This section describes the theory of operation for the logic analyzer and describes the self-tests. The information in this section is to help you understand how the logic analyzer operates and what the self-tests are testing. This information is not intended for component-level repair.

The block-level theory is divided into two parts: theory for the logic analyzer and theory for the acquisition boards. A block diagram is shown with each theory.

HP 1660CP-series analyzer theory



HP 1660CP-Series Logic Analyzer

CPU board

The microprocessor is a Motorola 68EC020 running at 25 MHz. The microprocessor controls all of the functions of the logic analyzer including processing and storing data, displaying data, and configuring the acquisition ICs to obtain and store data.

System memory

The system memory is made up of both read-only memory (ROM) and random access memory (RAM). Two types of ROM are used. A single 128Kx8 EPROM is used as a boot ROM, and four 512Kx8 Flash ROMs are configured to provide a 512Kx32 Flash ROM space. One SIMM socket supports 2-MB, 4-MB, or 8-MB SIMMs.

On power-up, instructions in the boot ROM command the instrument to execute its boot routine. The boot routine includes power-up operation verification of the instrument subsystems and entering the operating system. The CPU searches for the operating system on Flash ROM. Then, if the operating system is in Flash ROM, the instrument will be initialized with the default configuration and await front panel instructions from you. If the operating system is not in Flash ROM, the CPU accesses the disk drives to see if the operating system is on the disks.

The DRAM stores the instrument configuration, acquired data to be processed, and any inverse assembler loaded in the instrument.

Keypad and knob interface

The front panel keypad is scanned directly from the microprocessor address bus during the video blanking cycle of the CRT. When a front panel key is pressed, the associated address bits are fed to the data bus through the pressed key and read by the microprocessor.

The rotary pulse generator (RPG) knob is part of the PS2 circuitry. Pulses and direction of rotation information are directed to the RPG interface. The microprocessor then reads and interprets the RPG signals and performs the desired tasks.

HP-IB interface

The instrument interfaces to HP-IB as defined by IEEE Standard 488.2. The interface consists of an HP-IB controller and two octal drivers/receivers. The microprocessor routes HP-IB data to the controller. The controller then buffers the 8-bit HP-IB data bits and generates the bus handshaking signals. The data and handshaking signals are then routed to the HP-IB bus through the octal line drivers/receivers. The drivers/receivers provide data and control signal transfer between the bus and controller.

RS-232-C interface

The instrument RS-232-C interface is compatible with standard RS-232-C protocol. The interface consists of a controller and drivers/receivers. The controller serializes parallel data from the microprocessor for transmission. At the same time the controller also receives serial data and converts the data to parallel data characters for the microprocessor.

The controller contains a baud rate generator that can be programmed from the logic analyzer front panel. Other RS-232-C communications parameters can also be programmed from the logic analyzer front panel.

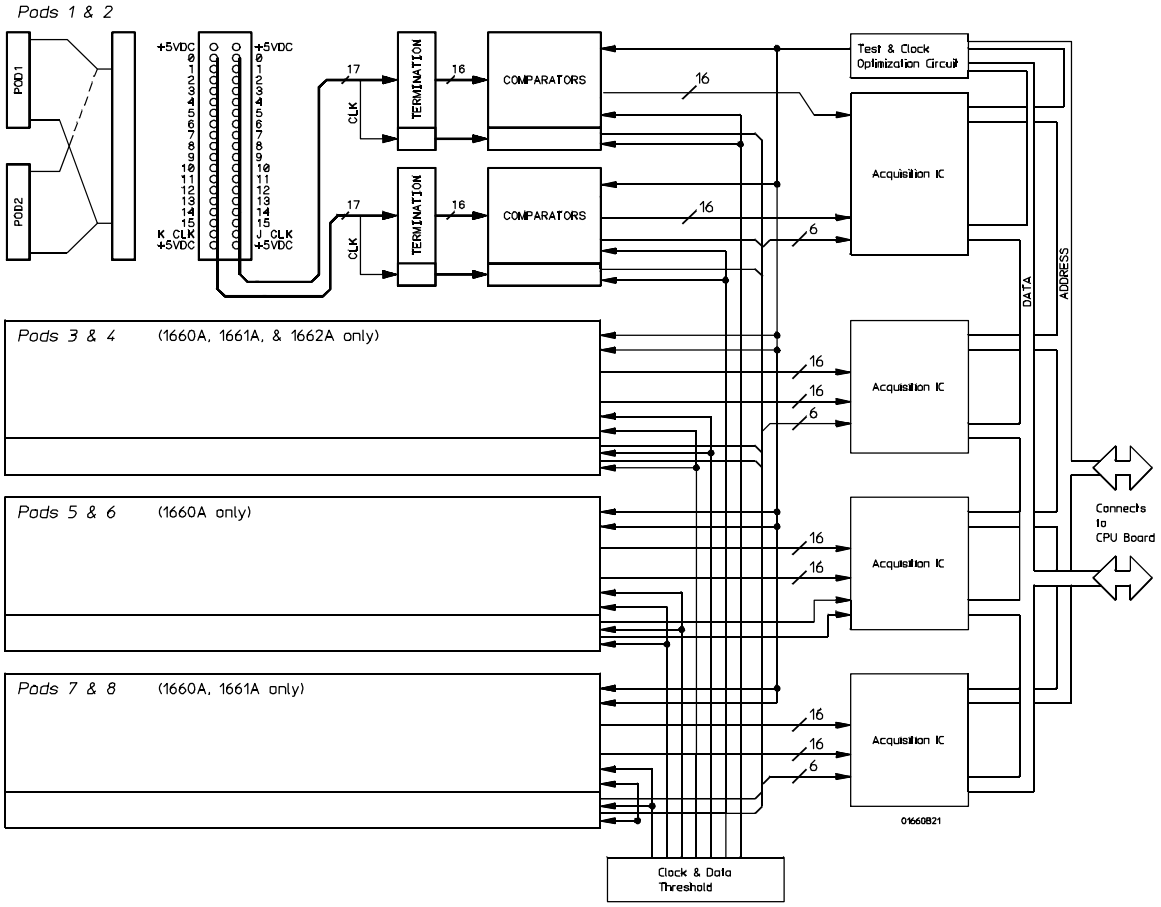
The drivers/receivers interface the instrument with data communications equipment. Slew rate control is provided on the ICs, eliminating the need for external capacitors.

Power supply

A low voltage power supply provides all dc voltages needed to operate the logic analyzer. The power supply also provides the +5 V dc voltage to the probe cables to power logic analyzer accessories and preprocessors.

Unfiltered voltages of +12 V, -12 V, +5 V, -5.2 V, and +3.5 V are supplied to the acquisition board where they are filtered and distributed to the CPU board, CRT monitor assembly, and probe cables.

Logic acquisition board theory



Logic Acquisition Board

Probing

The probing circuit includes the probe cable and terminations. The probe cable consists of two 17-channel pods which are connected to the circuit board using a high-density connector. Sixteen single-ended data channels and one single-ended clock/data channel per pod are passed to the circuit board. If the clock/data channel is not used as a state clock in state

acquisition mode, it is available as a data channel. The clock/data channel is also available as a data channel in timing acquisition mode. Eight (HP 1660CP), six (HP 1661CP), four (HP 1662CP), or two (HP 1663CP) clock/data channels are available as data channels; however, only six clock/data channels can be assigned as clock channels in the HP 1660CP and HP 1661CP. All clock data channels available in the HP 1662CP and HP 1663CP can be assigned as clock channels.

The cables use nichrome wire woven in polyarmid yarn for reliability and durability. The pods also include one ground path per channel in addition to a pod ground. The channel grounds are configured such that their electrical distance is the same as the electrical distance of the channel. The probe tip assemblies and termination modules connected at the end of the probe cables have a divide-by-10 RC network that reduces the amplitude of the data signals as seen by the circuit board. This adds flexibility to the types of signals the circuit board can read in addition to improving signal integrity.

The terminations on the circuit board are resistive terminations that reduce transmission line effects on the cable. The terminations also improve signal integrity to the comparators by matching the impedance of the probe cable channels with the impedance of the signal paths of the circuit board. All 17 channels of each pod are terminated in the same way. The signals are reduced by a factor of 10.

Comparators

Two proprietary 9-channel comparators per pod interpret the incoming data and clock signals as either high or low depending on where the user-programmable threshold is set. The threshold voltage of each pod is individually programmed, and the voltage selected applies to the clock channel as well as the data channels of each pod.

Each of the comparator ICs has a serial test input port used for testing purposes. A test bit pattern is sent from the Test and Clock Synchronization Circuit to the comparator. The comparators then propagate the test signal on each of the nine channels of the comparator. Consequently, all data and clock channel pipelines on the circuit board can be tested by the operating system software from the comparator.

Acquisition

The acquisition circuit is made up of a single HP-proprietary ASIC. Each ASIC is a 34-channel state/timing analyzer, and one such ASIC is included for every two logic analyzer pods. All of the sequencing, pattern/range recognition, and event counting functions are performed on board the IC.

In addition to the storage qualification and counting functions, the acquisition ASICs also perform master clocking functions. All six state acquisition clocks are fed to each IC, and the ICs generate their own sample clocks. Every time you select RUN, the ICs individually perform a clock optimization before data is stored.

Clock optimization involves using programmable delays on board the IC to position the master clock transition where valid data is captured. This procedure greatly reduces the effects of channel-to-channel skew and other propagation delays.

In the timing acquisition mode, an oscillator-driven clock circuit provides a four-phase, 100-MHz clock signal to each of the acquisition ICs. For high speed timing acquisition (100 MHz and faster), the sample period is determined by the four-phase, 100-MHz clock signal.

For slower sample rates, one of the acquisition ICs divides the 100-MHz clock signal to the appropriate sample rate. The sample clock is then fed to all acquisition ICs.

Threshold

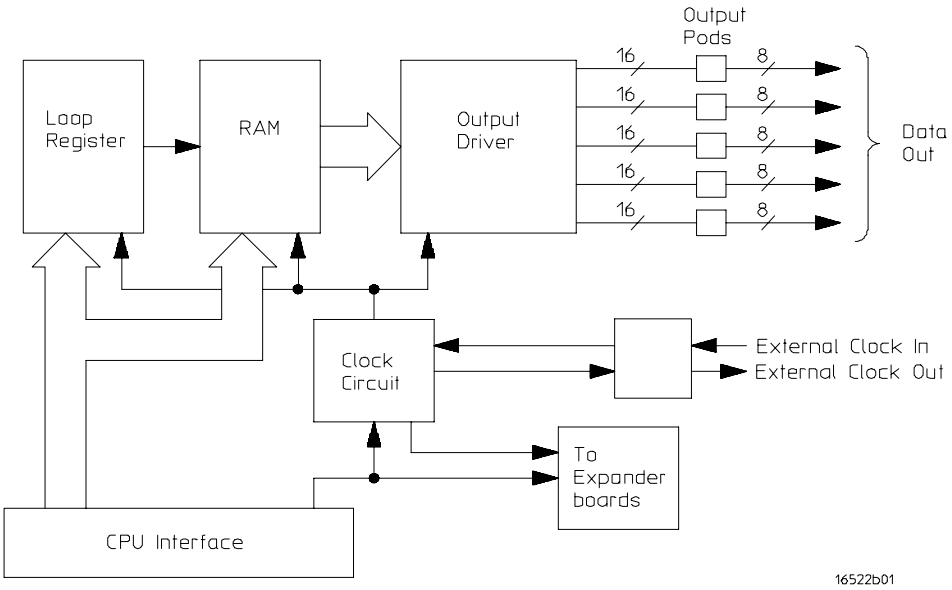
A precision octal DAC and precision op amp drivers make up the threshold circuit. Each of the eight channels of the DAC is individually programmable which allows you to set the thresholds of the individual pods. The 16 data channels and the clock channel of each pod are all set to the same threshold voltage.

Test and clock synchronization circuit

ECLinPS ICs are used in the test and clock synchronization circuit for reliability and low channel-to-channel skew. Test patterns are generated and sent to the comparators during software operation verification. The test patterns are propagated across all data and clock channels and read by the acquisition ASIC to ensure both the data and clock pipelines are operating correctly.

The test and clock synchronization circuit also generates a four-phase, 100-MHz sample/synchronization signal for the acquisition ICs operating in the timing acquisition mode. The synchronizing signal keeps the internal clocking of the individual acquisition ASICs locked in step with the other ASICs at fast sample rates. At slower sample rates, one of the acquisition ICs divides the 100-MHz clock signal to the appropriate sample rate. The slow speed sample clock is then used by all acquisition ICs.

Pattern Generator board theory



Pattern Generator Board

Loop Register

The loop register holds the programmable vector flow information. When the module reaches the end of the vector listing, the loop register is queried for the RAM address location of the next user-programmed vector. In many cases, the next vector address location would be the start of the vector listing. Consequently, the vectors would continue to loop from the end of the listing back to the beginning until you instruct the module to stop.

RAM

Consisting of five 256Kx16 VRAM ICs and RAM addressing circuitry, the RAM stores the desired patterns that appear at the module output. The RAM addressing circuitry is merely a counter which addresses the pattern locations in RAM. When the end of the vector listing is reached, the addressing circuitry is loaded from the loop register with the address of the first vector of the listing to provide an uninterrupted vector loop. The RAM output is sent to the Output Driver circuit where the patterns are presented in a logic configuration usable by the output pods.

Output Driver

The output driver circuit is made up of a series of latch/logic translators and multiplexers. The latch/translators convert the working-level TTL signals to output-level ECL signals for each channel. The ECL-level signals are then directed to the multiplexers.

The multiplexers, one per channel, direct the programmed data patterns to the output channels. The single-ended ECL-level signals are converted to differential signals which are routed to the output cables and to the pods. Note that the differential ECL output signal of the pattern generator module is not suitable to directly drive ECL circuitry.

Clock Circuit

The clock circuit paces the loop register, the RAM address circuitry, and the multiplexers in the output driver according to the desired data rate.
A 200 MHz clock source is directed through a divider circuit which provides a 100 MHz and 50 MHz clock in addition to 200 MHz. The 200 MHz, 100 MHz, 50 MHz and external clock signals are routed to a clock select multiplexer. The output of the multiplexer, which represents the user-selected clocking rate, is distributed to the above listed subcircuits.

The output of the clock select multiplexer is also distributed to an external clock out circuit. The clock signal is routed to a bank of external clock delays, and then to an external clock delay select multiplexer. The output of this multiplexer, which represents the desired clock delay, is directed to the external clock out pin on the clock pod. Consequently, either the internal clock or external clock is redirected to the clock out pin on the clock pod with a user-selected clock delay.

CPU Interface

The CPU interface is a single programmable-logic device which interprets the HP 1660CP Logic Analysis System backplane logic and translates the logic into signals to drive and program the pattern generator module.

Pod

The Clock or Data Pod converts the differential output ECL signal to the logic levels of interest. Because the output of the pattern generator module cannot directly drive ECL circuitry, the Clock and Data Pod is required to interface the pattern generator with the target system.

Self-tests description

The self-tests identify the correct operation of major functional areas in the logic analyzer. The self-tests are not intended for component-level diagnostics.

Three types of tests are performed on the HP 1660CP-series logic analyzers: the power-up self-tests, the functional performance verification self-tests, and the parametric performance verification tests.

The power-up self-tests are performed when power is applied to the instrument. The power-up self-tests are divided into two parts. The first part is the system memory tests and the second part is the microprocessor interrupt test. The system memory tests are performed before the logic analyzer actually displays the power-up self-test screen. Both the system ROM and RAM are tested during power-up. The interrupt test is performed after the power-up self-test screen is displayed.

The functional performance verification self-tests are run using a separate operating system, the performance verification (PV) operating system. The PV operating system resides on a separate disk that must be loaded when running the functional performance verification self-tests. The system and analyzer tests are functional performance verification tests.

Parametric performance verification requires the use of external test equipment that generates and monitors test data for the logic analyzer to read. Refer to the *HP 1660C/CS/CP-Series Logic Analyzers Service Guide* for further information about parametric performance verification.

Troubleshooting

Troubleshooting

Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes " ". Symptoms are listed without quotes.

If you still have difficulty using the analyzer after trying the suggestions in this chapter, please contact your local Hewlett-Packard Service Center.

CAUTION

When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and preprocessors. Otherwise, you may damage circuitry in the analyzer, preprocessor, or target system.

Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- ☐ **With the logic analyzer and all connected equipment turned off, remove and reseat all cables and probes; ensure that there are no bent pins on the preprocessor interface or poor probe connections.**

- ☐ **Adjust the threshold level of the data pod in the Format menu to match the logic levels in the system under test.**

- ☐ **Use an oscilloscope to check the signal integrity of the data lines.**

  Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also See "Capacitive loading" in this section for information on other sources of intermittent data errors.

Unwanted triggers

Unwanted triggers can be caused by instructions that were fetched but not executed.

- ☐ **Add the prefetch queue or pipeline depth to the trigger address.**

  The depth of the prefetch queue depends on the processor that you are analyzing. Suppose you are analyzing a pipelined processor having fetch, decode, execute, and memory stages. The processor fetches 32-bit words. To ensure that the processor has begun executing a particular routine when the

trigger occurs, set the trigger to the module entry address plus 08 hex. (This assumes that there is no immediate data in the instruction stream.)

No activity on activity indicators

- Ensure that the Threshold settings in the Format menu match the logic family being probed.
- Check for loose cables, board connections, and preprocessor interface connections.
- Check for bent or damaged pins on the preprocessor probe.

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the preprocessor interface, or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading, as can custom probe fixtures you design for your application. To reduce loading, remove as many pin protectors, extenders, and adapters as possible.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

No trace list display

If there is no trace list display, it may be that your trigger specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- Check your trigger specification to ensure that it will capture the events of interest.
- Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Preprocessor Problems

This section lists problems that you might encounter when using a preprocessor. If the solutions suggested here do not correct the problem, you may have a defective preprocessor. Refer to the User's Guide for your preprocessor for test procedures. Contact your local Hewlett-Packard Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the preprocessor interface, the microprocessor or the preprocessor interface may not be installed properly, or they may not be making electrical contact.

- ☐ **Ensure that you are following the correct power-on sequence for the preprocessor and target system.**

  1 Power up the analyzer and preprocessor.

  2 Power up the target system.

  If you power up the target system before you power up the preprocessor, interface circuitry in the preprocessor may latch up, preventing proper target system operation.

- ☐ **Verify that the microprocessor and the preprocessor interface are properly rotated and aligned, so that the index pin on the microprocessor (such as pin 1 or A1) matches the index pin on the preprocessor interface.**

- ☐ **Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.**

- ☐ **Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and are firmly inserted.**

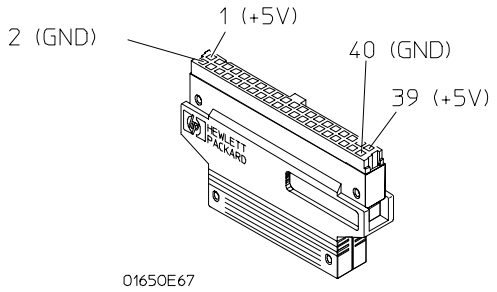
- ☐ **Reduce the number of extender sockets.**

See Also "Capacitive loading" in the previous section of this chapter.

Slow clock

If you have the preprocessor interface hooked up and running and observe a slow clock or no activity from the interface board, the +5 V supply coming from the analyzer may not be getting to the interface board.

☐ **To check the +5 V supply coming from the analyzer, disconnect one of the logic analyzer cables from the preprocessor and measure across pins 1 and 2 or pins 39 and 40.**



- If +5 V is not present, check the internal preprocessor fuse or current limiting circuit on the logic analyzer. For information on checking this fuse or circuit, refer to the *HP 1660C/CS/CP Logic Analyzers Service Guide*.
- If +5 V is present and the cable connection to the preprocessor appears sound, contact your nearest Hewlett-Packard Sales Office for information on servicing the board.

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and inverse assembly failures.

- ☐ **Ensure that the preprocessor configuration switches are correctly set for the measurement you are trying to make.**

  Some preprocessors include configuration switches for various features (for example, to allow dequeueing of the trace list). See your *Preprocessor User's Guide* for more information.

- ☐ **Try doing a full reset of the target system before beginning the measurement.**

  Some preprocessor designs require a full reset to ensure correct configuration.

- ☐ **Ensure that your target system meets the timing requirements of the processor with the preprocessor probe installed.**

  See "Capacitive loading" in this chapter. While preprocessor loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has poor timing margins, such loading may cause incorrect processor functioning, giving erratic trace results.

- ☐ **Ensure that you have sufficient cooling for the preprocessor probe.**

  Current processors such as the i486, Pentium™, and MC68040 generate substantial heat. This is exacerbated by the active circuitry on the preprocessor board. You should ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

Inverse Assembler Problems

This section lists problems that you might encounter while using the inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the preprocessor or in your target system. If you follow the suggestions in this section to ensure that you are using the preprocessor and inverse assembler correctly, you can proceed with confidence in debugging your target system.

No inverse assembly or incorrect inverse assembly

This problem is due to incorrect synchronization, modified configuration, incorrect connections, or a hardware problem in the target system. A locked status line can cause incorrect or incomplete inverse assembly.

- **Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display (not at the input cursor) and pressing the Invasm key.**

  Because the inverse assembler works from the first line of the trace *display*, if you jump to the middle of a trace and select Invasm, prior trace states are not disassembled correctly. If you move to several random places in the trace list and select Invasm each time, the trace disassembly is only guaranteed to be correct from the top of the display forward for each selection.

See Also "The Inverse Assembler" in Chapter 3.

- **Ensure that each analyzer pod is connected to the correct preprocessor cable.**

  There is not always a one-to-one correspondence between analyzer pod numbers and preprocessor cable numbers. Preprocessors must supply address (ADDR), data (DATA), and status (STAT) information to the analyzer in a predefined order, so the cable connections for each preprocessor are often altered to support that need. Thus, one preprocessor might require that you connect cable 2 to analyzer pod 2, while another will

require you to connect cable 5 to analyzer pod 2. See the *User's Guide* for your preprocessor for further information.

- ☐ **Check the activity indicators for status lines locked in a high or low state.**

- ☐ **Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values.**

  These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. Some preprocessors also require other data labels; check your *Preprocessor User's Guide* for more information.

- ☐ **Verify that all microprocessor caches and memory managers have been disabled.**

  In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly, but it may be incorrect since some of the execution trace was not visible to the logic analyzer.

- ☐ **Verify that storage qualification has not excluded storage of all the needed opcodes and operands.**

Inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

- ☐ **Ensure that the inverse assembler is on the same disk as the configuration files you are loading.**

  Configuration files for the state analyzer contain a pointer to the location of the corresponding inverse assembler. If you delete the inverse assembler or move it to another location, the configuration process will fail.

- ☐ **Make sure you are using the version of the inverse assembler software that corresponds to the operating system revision installed on your analyzer.**

  See your *Preprocessor User's Guide* for details.

Error Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted, and that it is on the same flexible disk or in the same directory as the configuration file.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module or the system into a different type of module.

- ☐ **Verify that the appropriate module has been selected as the target of the Load operation. Selecting Load All will cause incorrect operation when loading most preprocessor interface configuration files.**

See Also "To Load a Measurement Configuration" in chapter 7, "File Management."

"Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading a translatable configuration file for your logic analyzer.

"Slow or Missing Clock"

- ☐ This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.
- ☐ Check your State clock configuration. The proper clocking scheme should be listed in your preprocessor interface User's Guide.
- ☐ If the error message persists, check that the logic analyzer pods are connected to the proper connectors. See the User's Guide for your preprocessor interface to determine the proper connections.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

- ☐ When analyzing microprocessors that fetch only from long-word aligned addresses, if the trigger condition is set to look for an opcode fetch at an address not corresponding to a long-word boundary, the trigger will never be found.

"Must have at least 1 edge specified"

You must assign at least one clock edge to one of the available clocks in the clocking arrangment. The analyzer will not let you close the clock assignment pop-up until an edge is specified.

"Time correlation of data is not possible"

To time-correlate data, the data must be stored with time tags.

- Set the Count field in the Analyzer Trigger menu to Time.

"Maximum of 32 channels per label"

You have tried to assign more than 32 channels to a single label.

- Unassign some of the channels. If you need more than 32 channels to specify trigger conditions, you can AND terms in the Analyzer Trigger menu.

"Timer is off in sequence level n where it is used"

If you use timers as part of your trigger sequence, you must remember to turn them on using Timer Control in the Sequence Level pop-up menu.

- ☐ Check that your timers are turned on. The timer status is shown in the right side of the Sequence Level display of the Trigger menu. An "S" means "Start", "P" means "Pause", "C" means "Continue", and "-" means "off".

"Timer is specified in sequence, but never started"

This message often appears with "Timer is off in sequence level n where it is used," but is not quite the same. That message refers to a particular sequence level, but this message is a general warning that the timer has not been set to Start in any level.

- ☐ Start the timer in one of the levels before where it is used.

"Inverse assembler not loaded - bad object code."

The inverse assembler file has been corrupted.

- ☐ Try loading a different copy of the inverse assembler.

"Measurement Initialization Error"

The logic analyzer failed its internal hardware calibration.

- ☐ Run the Performance Verification tests.

See Also

Chapter 13, "Operator's Service," or the *HP 1660C/CS/CP-Series Logic Analyzers Service Guide* for information on running the Performance Verification test.

"Warning: Run HALTED due to variable change"

This message appears when certain analyzer settings are changed during a repetitive run. When this occurs, the analyzer stops.

Specifications

General Information

This chapter lists the accessories, specifications and characteristics for the HP 1660CP-series logic analyzers.

Accessories

The following accessories are supplied with the HP 1660CP-series logic analyzers. The part numbers are current as of this edition of the User's Guide, but future upgrades may change the part numbers. Do not be concerned if the accessories you receive have different part numbers.

Accessories supplied	**HP part number**	**Qty**
Probe tip assemblies	01650-61608	Note 1
Probe cables	01660-61605	Note 2
Grabbers (20 per pack)	5090-4356	Note 1
Probe ground (5 per pack)	5959-9334	Note 1
Logic Analyzer Training Kit	E2433-60009	1
HP 1660CP User's Guide	01660-99016	1
Symbol Utility (disk and manual)	E2450A	1
Accessories pouch	01660-84501	1
RS-232-C loopback connector	01650-63202	1
PS2 mouse	A2839B	1

Note 1 Quantities:
- 8 - 1660CP
- 6 - 1661CP
- 4 - 1662CP
- 2 - 1663CP

Note 2 Quantities:
- 4 - 1660CP
- 3 - 1661CP
- 2 - 1662CP
- 1 - 1663CP

Specifications (logic analyzer)

The specifications are the performance standards against which the product is tested. Refer to the *HP 1660C/CS/CP Logic Analyzers Service Guide* (available from your HP Sales Office) for testing procedures.

Maximum state speed	100 MHz
Minimum state clock pulse width*	3.5 ns
Minimum master-to-master clock time*	10.0 ns
Minimum glitch width*	3.5 ns
Threshold accuracy	± (100 mV + 3% of threshold setting)
Setup/Hold Time:*	
Single clock, single edge	0.0/3.5 ns through 3.5/0.0 ns, adjustable in 500-ps increments
Single clock, multiple edges	0.0/4.0 ns through 4.0/0.0 ns, adjustable in 500-ps increments
Multiple clocks, multiple edges	0.0/4.5 ns through 4.5/0.0 ns, adjustable in 500-ps increments

* Specified for an input signal VH = –0.9 V, VL = –1.7 V, slew rate = 1 V/ns, and threshold = –1.3 V.

Characteristics (logic analyzer)

These characteristics are not specifications, but are included as additional information.

		Full Channel	**Half Channel**
Maximum state clock rate		100 MHz	100 MHz
Maximum conventional timing rate		250 MHz	500 MHz
Maximum transitional timing rate		125 MHz	250 MHz
Maximum timing with glitch rate		N/A	125 MHz
Memory depth		4K	8K*
Channel count:			
	HP 1660CP	136	68
	HP 1661CP	102	51
	HP 1662CP	68	34
	HP 1663CP	34	17

* For all modes except glitch.

Characteristics (pattern generator)

These characteristics are not specifications, but are included as additional information.

	Full Channel	**Half Channel**
Channel count	32	16
Maximum speed	100 MHz	200 MHz
Memory depth	258,048	258,048

Logic levels	TTL, 3-state, TTL/3.3v, 3-state TTL/CMOS, ECL terminated, ECL Unterminated, and differential ECL (without POD)
Data inputs	3-bit pattern - level sensing (clock pod)
Clock outputs	Synchronized to output data
Clock input	DC to 200 MHz
Internal clock period	Programmable from 5 ns to 250 us in a 1, 2, 2.5, 4, 5, 8 sequence
External clock period (user supplied)	DC to 200 MHz
External duty cycle	2 ns minimum high time
Maximum number of "IF condition" blocks at 50 MHz	1
Maximum number for different Macros	100
Maximum number of lines in a Macro	1024
Maximum number of Macro invocations	1000
Maximum number of repeat loop invocations	1000
Maximum number of Wait event patterns	4

Supplemental characteristics (logic analyzer)

Probes

Input resistance	100 kΩ, ± 2%
Input capacitance	~ 8 pF
Minimum voltage swing	500 mV, peak-to-peak
Threshold range	± 6.0 V, adjustable in 50-mV increments, CAT I

State analysis

State/Clock qualifiers	1660/61CP - 6; 1662CP - 4; 1663CP - 2
Time tag resolution*	8 ns or 0.1%, whichever is greater
Maximum time count between states	34 seconds
Maximum state tag count*	4.29×10^9

Timing analysis

Sample period accuracy	0.01 % of sample period
Channel-to-channel skew	2 ns, typical
Time interval accuracy	± [sample period + channel-to-channel skew +(0.01%)(time reading)]

Triggering

Sequencer speed	125 MHz, maximum
State sequence levels	12
Timing sequence levels	10
Maximum occurrence counter value	1,048,575
Pattern recognizers	10
Maximum pattern width	136 channels in HP 1660CP, 102 channels in HP 1661CP, 68 channels in HP 1662CP, 34 channels in HP 1663CP
Range recognizers	2
Range width	32 bits each
Timers	2
Timer value range	400 ns to 500 seconds
Glitch/Edge recognizers	2 (timing only)
Maximum glitch/edge width	136 channels in HP 1660CP, 102 channels in HP 1661CP, 68 channels in HP 1662CP, 34 channels in HP 1663CP

* Maximum state clock rate with time or state tags on is 100 MHz. When all pods are assigned to a state or timing machine, time or state tags halve the memory depth.

Measurement and display functions

Displayed waveforms 24 lines maximum, with scrolling across 96 waveforms.

Measurement functions

Run/Stop functions Run starts acquisition of data in specified trace mode.

Stop In single trace mode or the first run of a repetitive acquisition, Stop halts acquisition and displays the current acquisition data. For subsequent runs in repetitive mode, Stop halts acquisition of data and does not change the current display.

Trace mode Single mode acquires data once per trace specification. Repetitive mode repeats single mode acquisitions until Stop is pressed or until the time interval between two specified patterns is less than or greater than a specified value, or within or not within a specified range.

Indicators

Activity indicators Provided in the Configuration and Format menus for identifying high, low, or changing states on the inputs.

Markers Two markers (X and O) are shown as vertical dashed lines on the display.

Trigger Displayed as a vertical dashed line in the Timing Waveform display and as line 0 in the State Listing display.

Data entry/display

Labels Channels may be grouped together and given a 6-character name. Up to 126 labels in each analyzer may be assigned with up to 32 channels per label.

Display modes State Listing, State Waveforms, Chart, Compare Listing, Compare Difference Listing, Timing Waveforms, and Timing Listings. State Listing and Timing Waveforms can be time-correlated on the same displays.

Timing waveform Pattern readout of timing waveforms at X or O marker.

Bases Binary, octal, decimal, hexadecimal, ASCII (display only), two's complement, and user-defined symbols.

Symbols 1,000 maximum. Symbols can be downloaded over RS-232 or HP-IB, or the optional LAN.

Marker functions

Time interval The X and O markers measure the time interval between a point on a timing waveform and the trigger, two points on the same timing waveform, two points on different waveforms, or two states (time tagging on).

Delta states (state analyzer only) The X and O markers measure the number of tagged states between one state and trigger or between two states.

Patterns The X and O markers can be used to locate the nth occurrence of a specified pattern from trigger, or from the beginning of data. The O marker can also find the nth occurrence of a pattern from the X marker.

Statistics X and O marker statistics are calculated for repetitive acquisitions. Patterns must be specified for both markers, and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum X to O time, maximum X to O time, average X to O time, and ratio of valid runs to total runs.

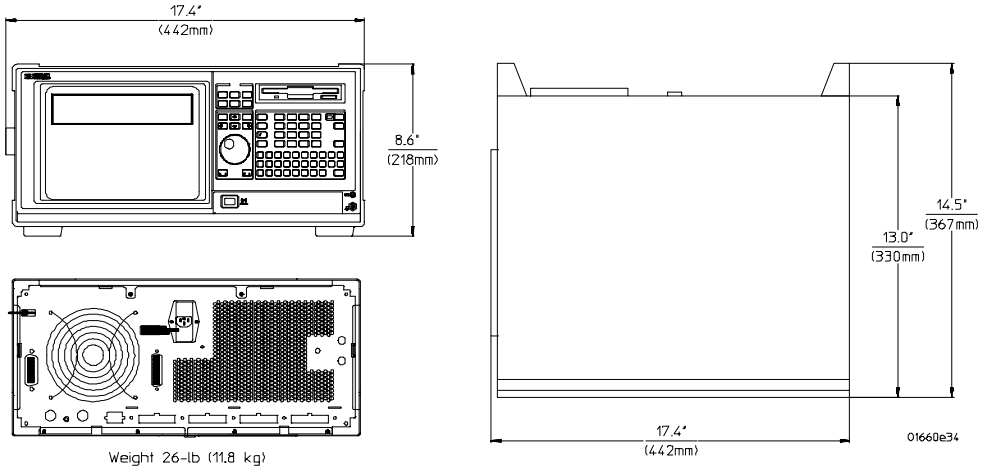
Auxiliary power

Power through cables	1/3 amp at 5 V maximum per cable

Operating environment

Temperature	Instrument, 0 °C to 55 °C (+32 °F to 131 °F). Probe lead sets and cables, 0 °C to 65 °C (+32 °F to 149 °F). Flexible disk media, 10 °C to 40 °C (+50 °F to 104 °F)
Humidity	Instrument, probe lead sets, and cables, up to 80% relative humidity at +40 °C (+122 °F).

Altitude	To 3067 m (10,000 ft).
Vibration	Operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈0.3 g (rms).
	Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈ 2.41 g (rms); and swept sine resonant search, 5 to 500 Hz, 0.75 g (0-peak), 5 minute resonant dwell at 4 resonances per axis.



Dimensions

Operator's Service

Operator's Service

This chapter provides information on how to prepare the logic analyzer for use, and contains self-tests and flow charts used for troubleshooting the logic analyzer.

The *HP 1660C/CS/CP-Series Logic Analyzers Service Guide* contains detailed service procedures. Service guides can be ordered through your HP Sales Office; they are not shipped with the logic analyzer.

This section gives you instructions for preparing the logic analyzer for use.

Power requirements

The logic analyzer requires a power source of either 115 VAC or 230 VAC, –22 % to +10 %, single phase, 48 to 66 Hz, 200 Watts maximum power.

Operating environment

The operating environment is listed in chapter 12. Note the noncondensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Provide protection against internal condensation.

The logic analyzer will operate at all specifications within the temperature and humidity range given in chapter 12. However, reliability is enhanced when operating the logic analyzer within the following ranges:

- Temperature: +20 °C to +35 °C (+68 °F to +95 °F)
- Humidity: 20% to 80% noncondensing

Storage

Store or ship the logic analyzer in environments within the following limits:

- Temperature: -40 °C to +75 °C
- Humidity: Up to 90% at 65 °C
- Altitude: Up to 15,300 meters (50,000 feet)

Protect the logic analyzer from temperature extremes which cause condensation on the instrument.

To inspect the logic analyzer

1. **Inspect the shipping container for damage.**

   If the shipping container or cushioning material is damaged, keep them until you have checked the contents of the shipment and checked the instrument mechanically and electrically.

2. **Check the supplied accessories.**

   Accessories supplied with the logic analyzer are listed in "Accessories" in chapter 12.

3. **Inspect the product for physical damage.**

   Check the logic analyzer and the supplied accessories for obvious physical or mechanical defects. If you find any defects, contact your nearest Hewlett-Packard Sales Office. Arrangements for repair or replacement are made, at Hewlett-Packard's option, without waiting for a claim settlement.

To apply power

1. **Check that the line voltage selector, located on the rear panel, is on the correct setting and the correct fuse is installed.**

   See also, "To set the line voltage" on the next page.

2. **Connect the power cord to the instrument and to the power source.**

   This instrument is equiped with a three-wire power cable. When connected to an appropriate ac power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination.

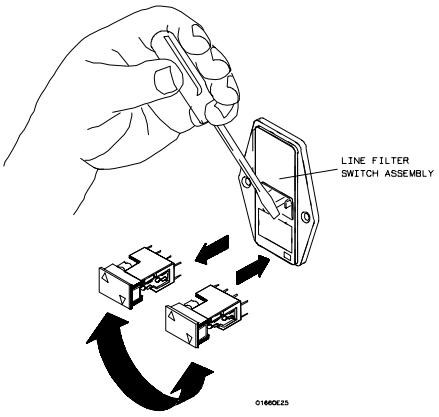
3. **Turn on the instrument power switch located on the front panel.**

To set the line voltage

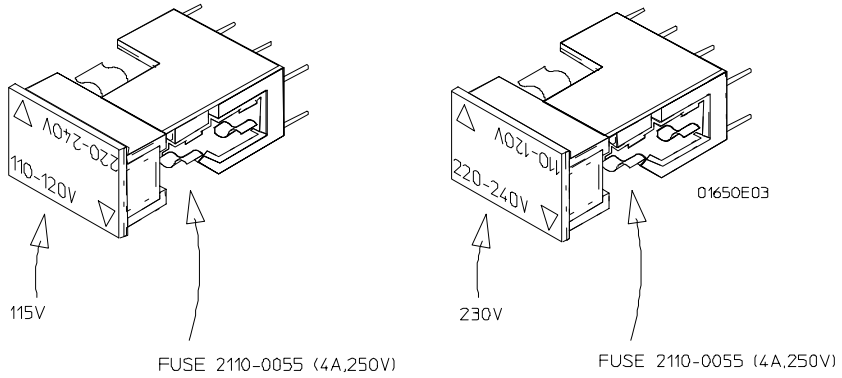
When shipped from HP, the line voltage selector is set and an appropriate fuse is installed for operating the instrument in the country of destination.

CAUTION Electrostatic discharge can damage electronic components. Use grounded wrist straps and mats when performing any service to the logic analyzer.

1. Turn the power off, then remove the power cord from the analzyer.
2. Remove the fuse module by carefully prying at the top center of the fuse module until you can grasp it and pull it out by hand.



3. Re-insert the fuse module with the arrow for the appropriate line voltage aligned with the arrow on the line filter assembly switch.



4. Reconnect the power cord and turn the analyzer on.

To degauss the display

If the logic analyzer has been subjected to strong magnetic fields, the CRT might become magnetized and display data might become distorted.

- To correct this condition, degauss the CRT with a conventional external television type degaussing coil.

To clean the logic analyzer

- With the instrument turned off and unplugged, use mild soap and water to clean the front and cabinet of the logic analyzer.
  Harsh soap might damage the water-base paint. Do not immerse the logic analyzer in water.

To test the logic analyzer

- If you require a test to verify the specifications, the *HP 1660C/CS/CP Series Logic Analyzers Service Guide* is required.
- If you require a test to initially accept the operation, perform the self-tests described in Troubleshooting in this chapter.
- If the logic analyzer does not operate correctly, go to the flow charts provided in Troubleshooting in this chapter.

Troubleshooting

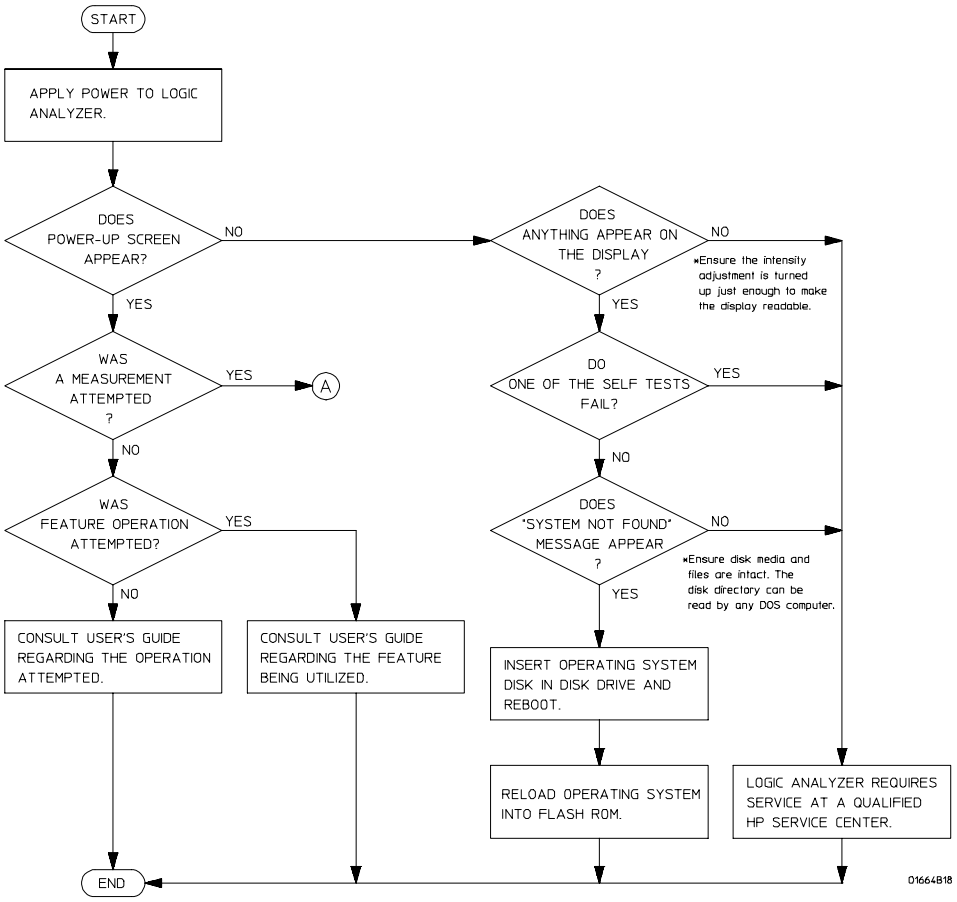
This section helps you troubleshoot the logic analyzer to find the problem. The troubleshooting consists of flowcharts, self-test instructions, and tests.

If you suspect a problem, start at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform other tests.

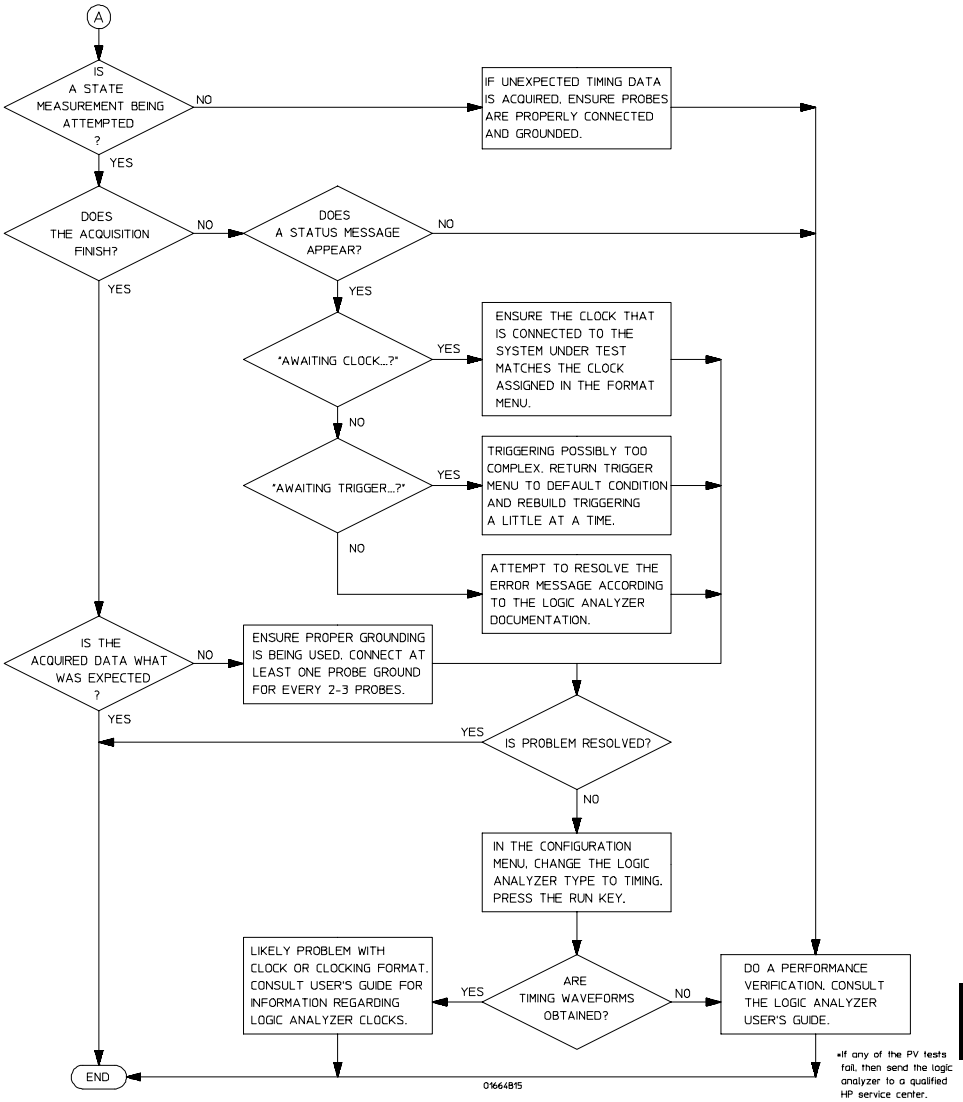
This instrument can be returned to Hewlett-Packard for all service work, including troubleshooting. Contact your nearest Hewlett-Packard Sales Office for more details.

To use the flowcharts

Flowcharts are the primary tool used to isolate problems in the logic analyzer. The flowcharts refer to other tests to help isolate the trouble. The circled letters on the charts indicate connections with the other flowcharts. Start your troubleshooting at the top of the first flowchart.



Troubleshooting Flowchart 1



Troubleshooting Flowchart 2

To check the power-up tests

The logic analyzer automatically performs power-up tests when you apply power to the instrument. The revision number of the operating system shows in the upper-right corner of the screen during these power-up tests. As each test completes, either "passed" or "failed" prints on the screen in front of the name of each test.

1. Disconnect all inputs, then insert a formatted disk into the flexible disk drive.
2. Let the analzyer warm up for a few minutes, then cycle power by turning off then turning on the power switch.

   If the analyzer is not warmed up, the power-up test screen will complete before you can view the screen.
3. As the tests complete, check if they pass or fail.

   The Flexible Disk Test reports No Disk if a disk is not in the disk drive.

Performing Power-Up Self-Tests

passed	ROM text
passed	RAM test
passed	Interrupt test
passed	Display test
passed	PS2 Controller Test
passed	Hard Disk Test
No Disk	Flexible Disk Test

To run the self-tests

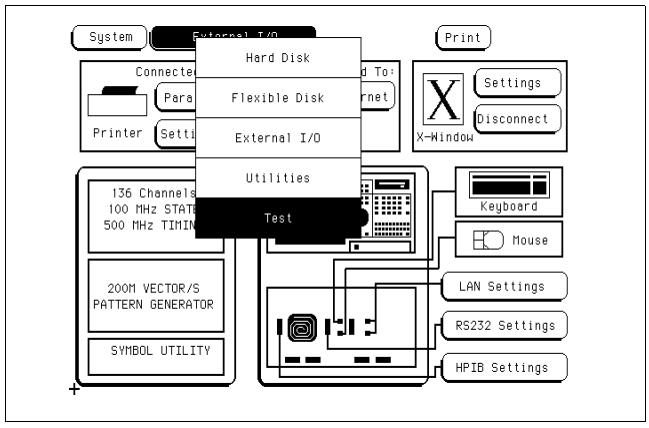
Self-tests identify the correct operation of major functional areas of the analyzer. You can run all self-tests without accessing the interior of the instrument. If a self-test fails, the troubleshooting flowcharts instruct you to change a part of the analzyer.

These procedures assume the files on the PV disk have been copied to the /SYSTEM subdirectory on the hard disk drive. If they have not already been copied, insert the PV disk in the flexible disk drive before starting this procedure.

1 If you just did the power-up self-tests, go to step 2.

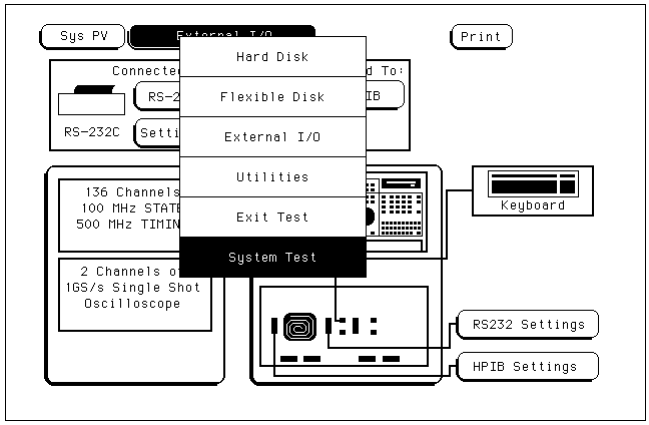
If you did not just do the power-up self-tests, disconnect all inputs, then turn on the power switch. Wait until the power-up tests are complete.

2 Press the System key, then select the field next to System. Then, select Test in the pop-up menu.



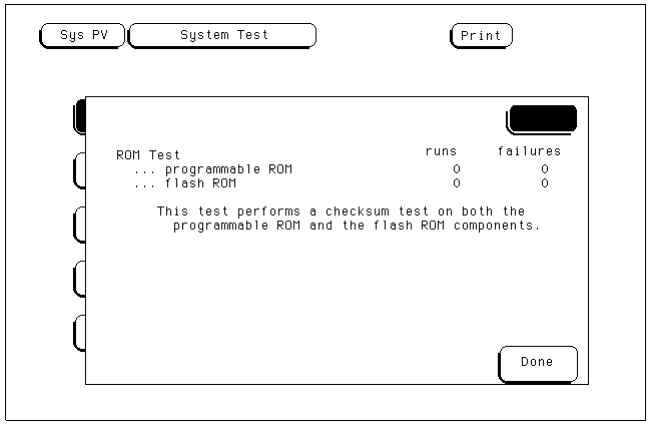
3 Select the box labeled Load Test System, then select Continue.

4 Press the System key, then select the field next to Sys PV. Select System Test to access the system tests.



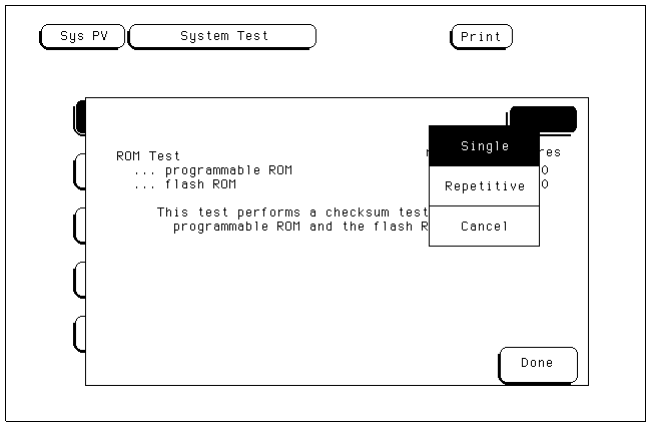
5 Select ROM Test. The ROM Test screen is displayed.

You can run all tests at one time by running All System Tests. To see more details about each test, you can run each test individually. This example shows how to run an individual test.

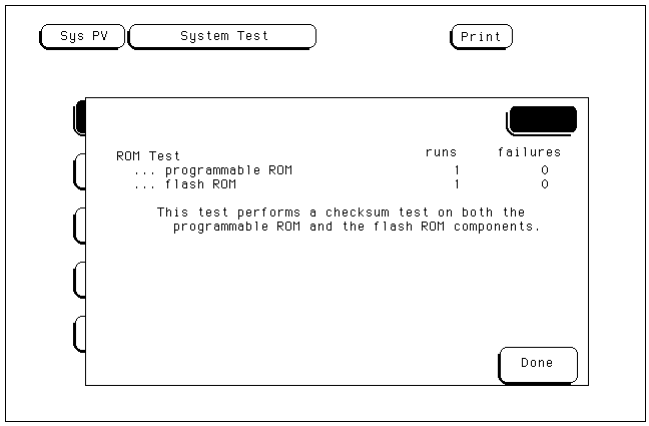


6 Select Run, then select Single.

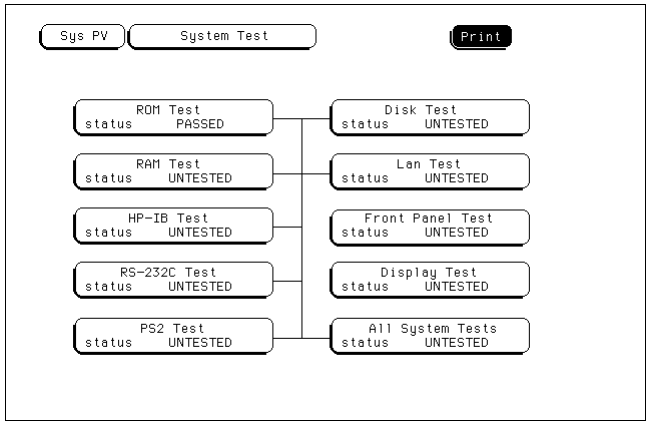
To run a test continuously, select Repetitive. Select Stop to halt a repetitive test.



For a Single run, the test runs one time, and the screen shows the results.



7 To exit the ROM Test, select Done. Note that the status changes to PASSED or FAILED.



8 Install a formatted disk that is not write-protected into the flexible disk drive. Connect an RS-232-C loopback connector onto the RS-232-C port. Run the remaining System Tests in the same manner.

9 Select the Front Panel Test.

A screen duplicating the front panel appears on the screen.

a Press each key on the front panel. The corresponding key on the screen will change from a light to a dark color.

b Test the knob by turning it in both directions.

c Note any failures, then press the Done key a second time to exit the Front Panel Test. The test screen shows the Front Panel Test status changed to TESTED.

10 Select the Display Test.

A white grid pattern is displayed. These display screens can be used to adjust the display.

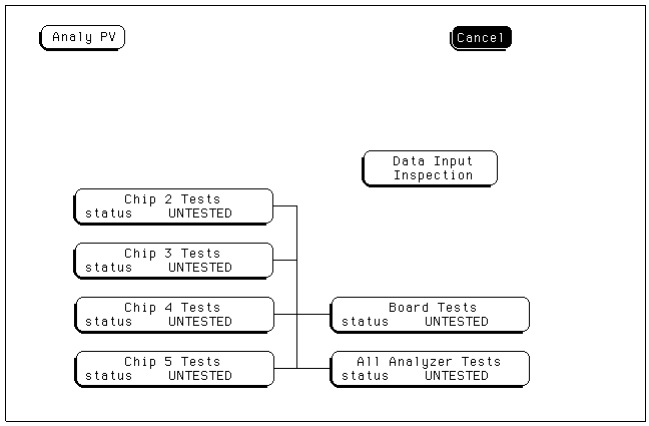
a Select Continue and the screen changes to full bright.

b Select Continue and the screen changes to half bright.

c Select Continue and the test screen shows the Display Test status changed to TESTED.

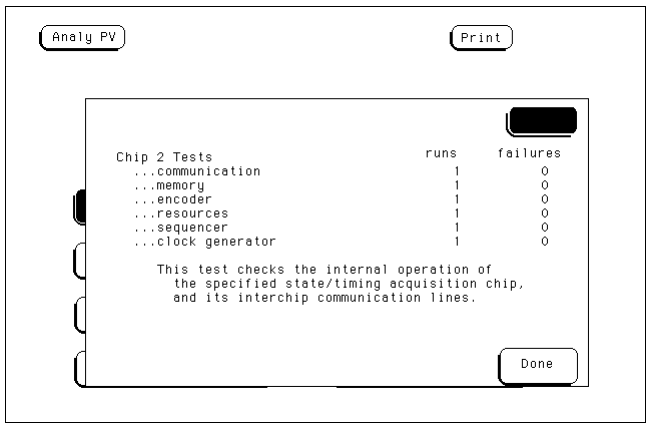
11 Select Sys PV, then select Analy PV in the pop-up menu. Select Chip 2 Tests.

You can run all the analyzer tests at one time by selecting All Analyzer Tests. To see more details about each test, you can run each test individually. This example shows how to run Chip 2 Tests. Chip 3, 4, and 5 Tests operate the same as Chip 2 Tests.

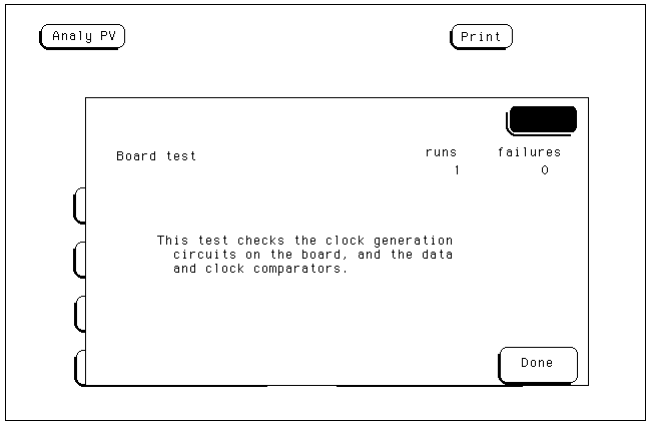


12 In the Chip 2 Tests menu, select Run, then select Single. The test runs one time, then the screen shows the results. When the test is finished, select Done. Then, perform the other Chip Tests.

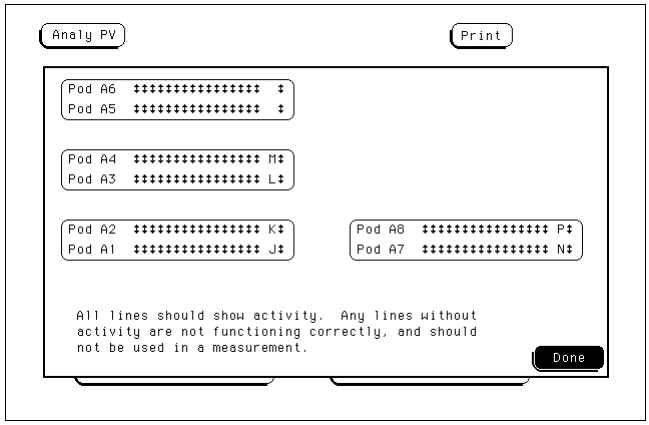
To run a test continuously, select Repetitive. Select Stop to halt a Run Repetitive.



13 Select Board Tests, then select Run. When the Board Tests are finished, select Done.



14 Select Data Input Inspection. All lines should show activity. Select Done to exit the Data Input Inspection.



15 To exit the tests, press the System key. Select the field to the right of the Sys PV field.

16 Select the Exit Test System.

If you are performing the self-tests as part of the troubleshooting flowchart, return to the flowchart.

To test the auxiliary power

The +5 V auxiliary power is protected by a current overload protection device. If the current on pins 1 and 39 exceeds 0.33 amps, the circuit will open. When the short is removed, the circuit will reset in approximately 1 minute. There should be +5 V after the 1 minute reset time.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	0.1 mV resolution, better than 0.005% accuracy	HP 3478A

- Using the multimeter, verify the +5 V on pins 1 and 39 of the probe cables.

Glossary

benchtop logic analyzer A small, standalone HP logic analyzer that operates independently from the HP 16500 logic analysis system.

bit The information the logic analyzer stores for one sample of one physical line. Bits are either "low" or "high." See also channel.

bucket In the SPA State Overview mode, an individual subrange of states displayed on the histogram's X axis.

channel The analyzer's mapping of a single physical line. Channel is often used interchangeably with bit. Channels are grouped into labels in the Analyzer Format menu.

don't care Signifies that the signal state should be ignored. "Don't cares" are represented by "X" in assignment fields.

glitch A pulse of very short duration, usually less than the setup or hold time. To the logic analyzer, a glitch is two or more transitions across the logic threshold between consecutive samples.

label A name for a group of functionally-related channels. Three common labels, which are required by HP preprocessor interface inverse assemblers, are ADDR, DATA, and STAT. If a label is on, it appears in all display menus and the Trigger menu, letting you quickly display, store, or trigger on information of interest. See also symbol and term.

listing An alphanumeric display of state information. See also trace and waveform.

menu field The field to the right of the mode field. The menu field lets you set up the instrument selected in the mode field.

mode field Also known as module field. The field in the upper-left corner of the logic analyzer. This field selects the mode, such as "Analyzer" or "System."

module field See mode field.

OMF Symbol Table OMF stands for Object Module File. The HP E2450A Symbol Utility uses the OMF to produce a table of symbols in the executable.

storage qualification Storage qualification allows you to specify the type of information to be stored in memory. Use storage qualification to prevent memory from being filled with unwanted activity.

symbol An alphanumeric name given to a specified bit-pattern or range for the bits in a particular label (see label). A label can have many symbols, each having a different meaning. For example, if the CYCLE label includes the bits for the Read/Write (R/W) and I/O signals, one symbol might be I/O READ, with I/O and R/W both high, while another symbol might be I/O WRITE, with I/O high and R/W low. Symbols are named and specified in the Format menu. Symbols are available only when the associated label is on. Symbols are also available for defining trigger terms. See also label and term.

term A resource for specifying storage conditions or trigger conditions. A term uses the bits in a label to identify the condition for storage or triggering. If symbols have previously been defined for the label, they can be used as the conditions, or you can specify new patterns or ranges. For example, if the CYCLE label includes the symbols I/O READ and I/O WRITE, term "a" could be I/O READ and term "b" could be I/O WRITE, and the trigger/storage macro could be to start storing at term "a" and stop storing at term "b."

trace The record of target system activity stored by the state or timing analyzer. This record can be displayed as either a waveform or a listing. See also listing and waveform.

trigger A reference event around which you want to gather information. In the analyzer, you might want to trigger on a glitch in hardware or entry to a subroutine in software. When beginning, you might want to trigger on the first occurrence of any kind (trigger on "anystate"). As you learn more about the problem you are trying to isolate, you may enter more specific trigger conditions. When you want to gather a continuous stream of activity leading up to a system crash, you will want to trigger on "no state." Note that some microprocessors fetch instructions on 32-bit boundaries. If you are tracing activity of one of these processors, and you specify trigger on an address that is not on a 32-bit boundary, that address will never appear on the address bus; therefore, the analyzer will never find its trigger. Make sure you specify triggers that the analyzer will find. The state

analyzer, timing analyzer, and oscilloscope cannot complete their measurement unless they find a trigger.

user symbol table A table containing the symbols that are created by the user, using the Symbols option in the Format menu. This is the standard symbol capability of the HP logic analyzer. See also OMF Symbol Table.

waveform An oscilloscope-like display of a trace. Because analyzers only record whether a line is "low" or "high" at the time of sampling, the waveforms are sharp square waves rather than the rough curves of an oscilloscope. See also listing and trace.

Index

Document Warranty

The information contained in this document is subject to change without notice.

Hewlett-Packard makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties or merchantability and fitness for a particular purpose.

Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this material.

Complete product warranty information is given on the last page of this guide.

Safety

This apparatus has been designed and tested in accordance with IEC Publication 348, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warning

- Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.
- Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.
- If you energize this instrument by an auto transformer (for voltage reduction), make sure the common terminal is connected to the earth terminal of the power source.
- Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.
- Use caution when exposing or handling the CRT. Handling or replacing the CRT shall be done only by qualified maintenance personnel.

Safety Symbols

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

WARNING

The Warning sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a Warning sign until the indicated conditions are fully understood and met.

CAUTION

The Caution sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a Caution symbol until the indicated conditions are fully understood or met.

Hewlett-Packard
P.O. Box 2197
1900 Garden of the Gods Road
Colorado Springs, CO 80901

Product Warranty

This Hewlett-Packard product has a warranty against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products that prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by Hewlett-Packard.

For products returned to Hewlett-Packard for warranty service, the Buyer shall prepay shipping charges to Hewlett-Packard and Hewlett-Packard shall pay shipping charges to return the product to the Buyer. However, the Buyer shall pay all shipping charges, duties, and taxes for products returned to Hewlett-Packard from another country.

Hewlett-Packard warrants that its software and firmware designated by Hewlett-Packard for use with an instrument will execute its programming instructions when properly installed on that instrument. Hewlett-Packard does not warrant that the operation of the instrument software, or firmware will be uninterrupted or error free.

Limitation of Warranty

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by the Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

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The remedies provided herein are the buyer's sole and exclusive remedies. Hewlett-Packard shall not be liable for any direct, indirect, special, incidental, or consequential damages, whether based on contract, tort, or any other legal theory.

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Certification

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology, to the extent allowed by the Institute's calibration facility, and to the calibration facilities of other International Standards Organization members.

About this edition

This is the first edition of the *HP 1660CP-Series Logic Analyzers User's Guide*

Publication number
01660-97023

Printed in USA.

Edition dates are as follows:

First edition, November 1997

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by you. The dates on the title page change only when a new edition is published.

A software or firmware code may be printed before the date. This code indicates the version level of the software or firmware of this product at the time the manual or update was issued. Many product updates do not require manual changes; and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.

The following list of pages gives the date of the current edition and of any changed pages to that edition.

All pages original edition

DECLARATION OF CONFORMITY

according to ISO/IEC Guide 22 and EN 45014

Manufacturer's Name: Hewlett-Packard Company

Manufacturer's Address: Colorado Springs Division
1900 Garden of the Gods Road
Colorado Springs, CO 80907 USA

declares, that the product

Product Name: Logic Analyzer / Pattern Generator

Model Number(s): HP 1660CP, HP 1661CP, HP 1662CP and HP 1663CP

Product Option(s): All

conforms to the following Product Specifications:

Safety:	IEC 1010-1:1990+A1 / EN 61010-1:1993	
	UL 3111	
	CSA-C22.2 No. 1010.1:1993	
EMC:	CISPR 11:1990 / EN 55011:1991	Group 1 Class A
	IEC 555-2:1982 + A1:1985 / EN 60555-2:1987	
	IEC 555-3:1982 + A1:1990 / EN 60555-3:1987 + A1:1991	
	IEC 801-2:1991 / EN 50082-1:1992	4 kV CD, 8 kV AD
	IEC 801-3:1984 / EN 50082-1:1992	3 V/m, {1kHz 80% AM, 27-1000 MHz}
	IEC 801-4:1988 / EN 50082-1:1992	0.5 kV Sig. Lines, 1 kV Power Lines

Supplementary Information:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC and carries the CE marking accordingly.

This product was tested in a typical configuration with Hewlett-Packard test systems.

Colorado Springs, 11/10/97

Ken Wyatt

Ken Wyatt/Product Regulations Manager

European Contact: Your local Hewlett-Packard Sales and Service Office or Hewlett-Packard GmbH, Department ZQ / Standards Europe, Herrenberger Strasse 130, D-71034 Böblingen Germany (FAX: +49-7031-14-3143)

Product Regulations

Safety

IEC 1010-1:1990+A1 / EN 61010-1:1993
UL 3111
CSA-C22.2 No.1010.1:1993

EMC

This Product meets the requirement of the European Communities (EC) EMC Directive 89/336/EEC.

CE
ISM 1-A

Emissions EN55011/CISPR 11 (ISM, Group 1, Class A equipment)
IEC 555-2 and IEC 555-3

N279

Immunity

EN50082-1	Code[1]	Notes[2]
IEC 801-2 (ESD) 8kV AD	1	
IEC 801-3 (Rad.) 3V/m	1	
IEC 801-4 (EFT) 1kV	1	

[1] Performance Codes:
1 PASS - Normal operation, no effect.
2 PASS - Temporary degradation, self recoverable.
3 PASS - Temporary degradation, operator intervention required.
4 FAIL - Not recoverable, component damage.

[2] Notes: (none)

Sound Pressure Level Less than 60 dBA